EXHIBIT A

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
90/014,839	08/25/2021	7663615	034960.0038-US02	4670

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EXAMINER	
BONSHOCK, DENNIS G	

ART UNIT	PAPER NUMBER
3992	

MAIL DATE	DELIVERY MODE
02/17/2022	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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EX PARTE REEXAMINATION COMMUNICATION TRANSMITTAL FORM

REEXAMINATION CONTROL NO. *90/014,839* .

PATENT UNDER REEXAMINATION *7663615* .

ART UNIT *3992* .

Enclosed is a copy of the latest communication from the United States Patent and Trademark Office in the above identified *ex parte* reexamination proceeding (37 CFR 1.550(f)).

Where this copy is supplied after the reply by requester, 37 CFR 1.535, or the time for filing a reply has passed, no submission on behalf of the *ex parte* reexamination requester will be acknowledged or considered (37 CFR 1.550(g)).

Office Action in Ex Parte Reexamination	**Control No.** 90/014,839	**Patent Under Reexamination** 7663615	
	Examiner DENNIS G BONSHOCK	**Art Unit** 3992	**AIA (FITF) Status** No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

a. ☑ Responsive to the communication(s) filed on 23 December 2021.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

b. ☐ This action is made FINAL.

c. ☐ A statement under 37 CFR 1.530 has not been received from the patent owner.

A shortened statutory period for response to this action is set to expire 2 month(s) from the mailing date of this letter. Failure to respond within the period for response will result in termination of the proceeding and issuance of an *ex parte* reexamination certificate in accordance with this action. 37 CFR 1.550(d). **EXTENSIONS OF TIME ARE GOVERNED BY 37 CFR 1.550(c).** If the period for response specified above is less than thirty (30) days, a response within the statutory minimum of thirty (30) days will be considered timely.

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☐ Notice of References Cited by Examiner, PTO-892.
2. ☑ Information Disclosure Statement, PTO/SB/08.
3. ☐ Interview Summary, PTO-474.
4. ☐ _____.

Part II SUMMARY OF ACTION

1a. ☑ Claims 11-13 are subject to reexamination.

1b. ☑ Claims 1-10 and 14-15 are not subject to reexamination.

2. ☐ Claims _____ have been canceled in the present reexamination proceeding.

3. ☐ Claims _____ are patentable and/or confirmed.

4. ☑ Claims 11-13 are rejected.

5. ☐ Claims _____ are objected to.

6. ☐ The drawings, filed on _____ are acceptable.

7. ☐ The proposed drawing correction, filed on _____ has been (7a) ☐ approved (7b) ☐ disapproved.

8. ☑ Acknowledgment is made of the priority claim under 35 U.S.C. 119(a)-(d) or (f).

a) ☑ All b) ☐ Some* c) ☐ None of the certified copies have

1 ☐ been received.

2 ☐ not been received.

3 ☑ been filed in Application No. 11/302,590.

4 ☐ been filed in reexamination Control No. _____.

5 ☐ been received by the International Bureau in PCT application No. _____.

* See the attached detailed Office action for a list of the certified copies not received.

9. ☐ Since the proceeding appears to be in condition for issuance of an *ex parte* reexamination certificate except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte* Quayle, 1935 C.D. 11, 453 O.G. 213.

10. ☐ Other: _____

cc: Requester (if third party requester)

Notice of Pre-AIA or AIA Status

The present application is being examined under the pre-AIA first to invent provisions.

DECISION ON REQUEST FOR REEXAMINATION

A Non-Final Office Action affecting claims 11-13 of United States Patent Number: 7,663,615 issued to Shirasaki et al. (hereinafter the '615 patent). The '615 patent granted on 2/16/2010 from US application number: 11/302,590 (hereinafter the '590 application). A SNQ was raised by the Request for *ex parte* reexamination filed 8/25/2021. The Examiner Ordered reexamination on 10/7/2021. Responsive to the Office ordering reexamination, the Patent Owner chose to file a Patent Owner statement on 12/17/2021, with the Third Party Requester subsequently filing a Third Party Requester's Reply on 12/23/2021.

Extensions of time under 37 CFR 1.136(a) will not be permitted in these proceedings because the provisions of 37 CFR 1.136 apply only to "an applicant" and not to parties in a reexamination proceeding. Additionally, 35 U.S.C. 305 requires that *ex parte* reexamination proceedings "will be conducted with special dispatch" (37 CFR 1.550(a)). Extensions of time in *ex parte* reexamination proceedings are provided for in 37 CFR 1.550(c).

Information Disclosure Statement

The IDS submission(s) have been considered by the Examiner only with the scope required by MPEP 2256, unless otherwise noted.

MPEP 2256:

> *"Where patents, publications, and other such items of information are submitted by a party (patent owner) in compliance with the requirements of the rules, the requisite degree of consideration to be given to such information will be normally limited by the degree to which the party filing the information citation has explained the content and relevance of the information."*

Where the IDS citations are submitted but not described, the examiner is only responsible for cursorily reviewing the references. The initials of the examiner on the PTO-1449 indicate only that degree of review unless the reference is either applied against the claims, or discussed by the examiner as pertinent art of interest, in a subsequent office action.

See Guidelines for Reexamination of Cases in View of In re Portola Packaging, Inc., 110 F.3d 786, 42 USPQ2d 1295 (Fed. Cir. 1997), 64 FR at 15347, 1223 Off. Gaz. Pat. Office at 125 (response to comment 6).

References

(1) Kimura I / Ex. 3, U.S. Publication No.: 2003/0117352 (hereinafter "Kimura I")

(2) Kimura II / Ex. 14, U.S. Publication No.: 2004/0227749 (hereinafter "Kimura II")

(3) Dawson / Ex. 15, PCT Publication No.: WO 98/48403 (hereinafter "Dawson")

Prosecution History

Original Prosecution:

The patent application that issued as the '615 Patent was filed on December 12, 2005, as U.S. Patent Application No. 11/302,590 (the '590 Application").

2/11/2009 – Claims 1-17, 19-24, 33-35, and 37-50 were rejected under 35 U.S.C. 102(e) as being anticipated by Tsuge et al. (EP 1 434 193), while claims 18, 25-32, and 36 were noted to be objected to as being dependent upon a rejected base claim but would otherwise be allowable if rewritten in independent form including all of the limitation of the base claim and any intervening claims. Specifically, noting for dependent claim 29 that:

> *Relative to claim 29 the major difference between the teaching of the prior art of record (Tsuge et al.) and the instant invention is that the data driver applies a precharge voltage exceeding the threshold value of the drive transistor to the data line, and the light emission drive circuit applies the precharge voltage applied to the data line to the electric charge accumulating section via the writing control section.*

6/11/2009 – Patent Owner provided an amended claim set including amended claim 29, which moved each limitation from the parent claims (original claims 23 and 24) into now independent claim 29.

9/30/2009 and 11/4/2009 – Patent Office issued a Notice of Allowability renumbering claim 29 to allowed claim 11.

Litigation History

The subject patent of this Reexamination, the '615 Patent is involved in the following prior or concurrent litigation:

- Solas OLED Ltd. v. HP Inc., Case 6:19-cv-00631 (W.D. Texas) (filed October 24, 2019) ("HP Litigation") (Ex. 9).
- Solas OLED Ltd v. Samsung Display Co., Ltd., Case 2:21-cv-00104 (E.D. Texas) (filed March 22, 2021) (Ex. 5).
- Solas OLED Ltd. v. BOE Tech. Group Co., Ltd., Case No. 2:21-cv-00121 (E.D. Texas) (filed April 1, 2021) (Ex. 16).
- Samsung Elecs. Co., Ltd. v. Solas OLED Ltd., Case No. 1:21-cv-05205 (S.D. New York) (filed June 11, 2021) (Ex. 17).

Claim Rejections

In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

The following is a quotation of the appropriate paragraphs of pre-AIA 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

A. Kimura I

Claims 11-13 are rejected under pre-AIA 35 U.S.C. 102 (b) as anticipated by or, in the alternative, under pre-AIA 35 U.S.C. 103(a) as obvious over Kimura (Ex. 3), U.S. Publication No.: 2003/0117352 (hereinafter Kimura I), as presented on pages 30-35 and 39-73 of the Request and reproduced in part below.

With regard to claim 11, teaching (preamble) ***A display unit*** Kimura I teaches, referring to Figs. 17A—17H above, a variety of devices that comprise a display unit (i.e., the 'display portion" elements 3003, 3102, 3203, 3302, 3403, 3502, 3602, 3703). Ex. 3, Figs. 17A-17H, ¶¶ [0403]-[0412]. Each of the devices in Figs. 17A-17H are "examples of electronic devices to which the present invention can be applied." Id., ¶ [0162]

With regard to claim 11 teaching ***(a) the display unit comprising: a plurality of display pixels each of which includes a light emission element and a light emission drive circuit***, Kimura I discloses a "plurality of display pixels' (i.e., pixel portion 702):

FIG. 7A

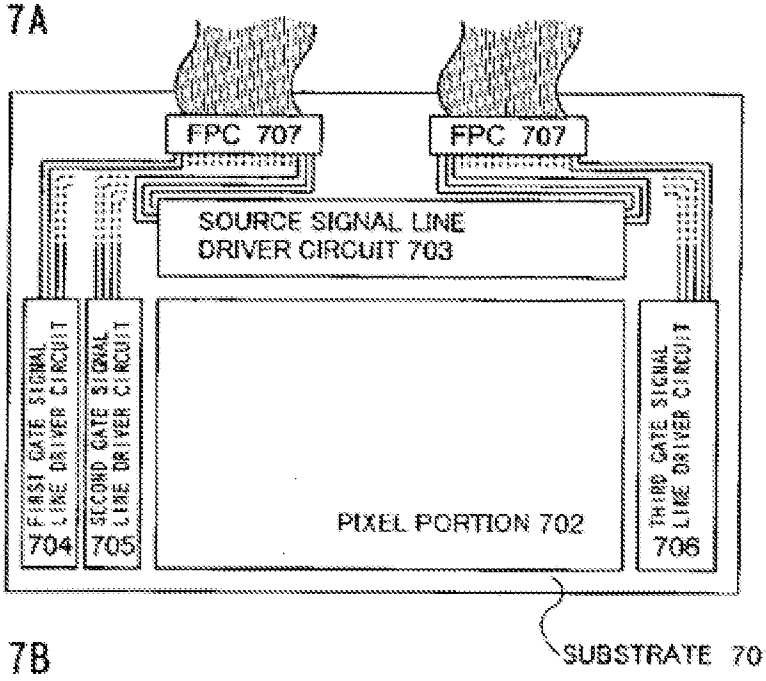
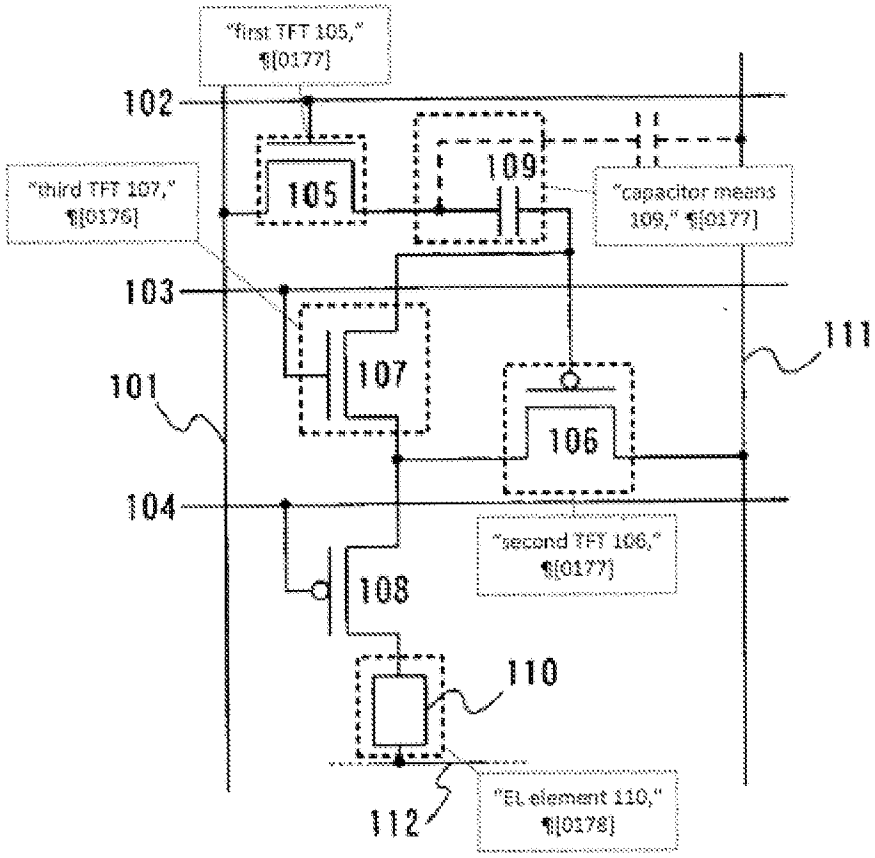


FIG. 7B

Ex. 3, Fig. 7A. Id., ¶ [0193] ("A configuration example of the semiconductor device is shown in FIG. 7A. The device has a pixel portion 702 wherein a plurality of pixels is arranged in a matrix shape over a substrate 701.") (emphasis added).

Kimura I discloses that each pixel (as shown in FIG. 1A) within pixel portion 702 "includes a light emission element and a light emission drive circuit":

FIG. 1A



Ex. 3, Fig. 1A (annotated).

Referring to annotations in Fig. 1 above, Kimura I discloses a "light emission element" as EL (i.e., electroluminescence) element 110. Ex. 3, [0178]; see also id., ¶ [0004]. When current flows into the EL element 110, it emits light. Ex. 3, ¶ [0185] ("Thus ...a current flows into the EL element so that the EL element emits light.").

Still referring to the annotations in Fig. 1 above, Kimura I discloses a "light emission drive circuit" that includes first to fourth TFTs 105 to 108 and capacitor means 109, which are all connected via wiring shown in the diagram above. Ex. 3, ¶¶ [0176]-[0178]. As shown in annotated Fig. 1 above, the light emission drive circuit is connected to the light emission element 110, as well as a source signal line 101, first to third gate lines 102 to 104 and current supply line 111. Id.

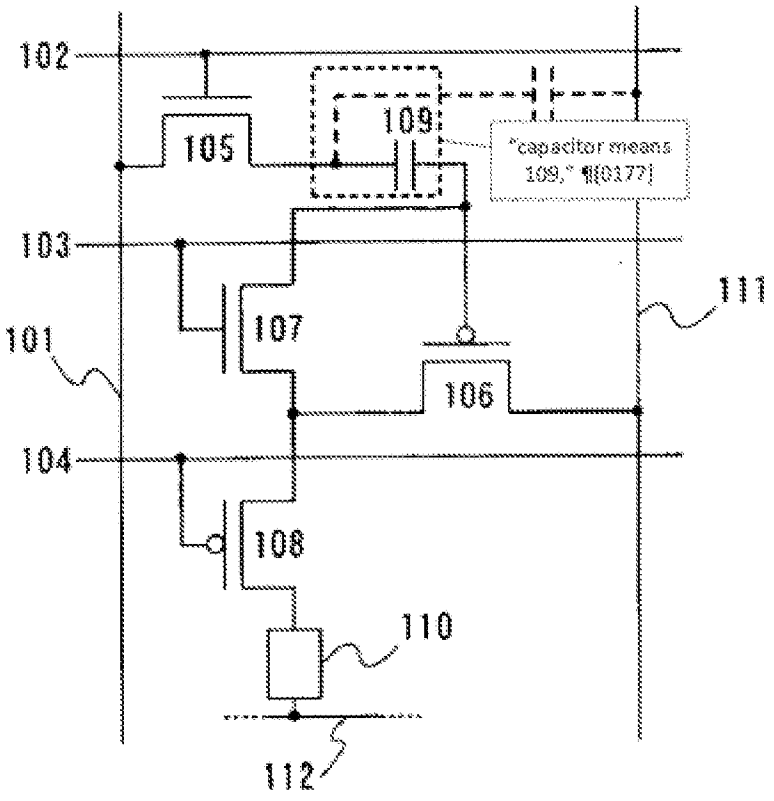
With regard to claim 11, ***further teaches (b) the light emission drive circuit having an electric charge accumulating section for accumulating electric charges based on a gradation sequence signal to designate a luminance gradation sequence in accordance with display data***,
Kimura I teaches this limitation. For convenience, limitation [11b] is addressed in three parts below.

<u>i. Kimura discloses an "electric charge accumulating section" as part of its "light emission drive circuit."</u>

As discussed in Section IX.A.7 of the Request, Requester submits that the broadest reasonable interpretation of the term "electric charge accumulating section" should include a capacitor, the Examiner agrees.

As shown in Fig. 1A below, Kimura I discloses an "electric charge accumulating section" (i.e., capacitor means 109) included in its light emission drive circuit (i.e., elements 105-109):

FIG. 1A



Ex. 3, Fig. 1A (annotated); see also id., ¶ [0176] ("A pixel includes . . capacitor means 109").

ii. Kimura discloses a "gradation sequence signal."

As discussed in Section IX.A.1 of the Request, Patent Owner previously agreed that the term "gradation" should be construed as "level."

Kimura discloses a sequence signal level, Vdata, corresponding to a video signal. Ex. 3, ¶ [0183] ("The video signal is outputted to the source signal line 101 and its potential is changed from VDD to a potential of the video signal Vdata").

Moreover, for the avoidance of doubt, as explained by Dr. Fontecchio, Kimura I discloses multiple methods to generate a Vdata signal, including an "analog gradation method" and a "digital time gradation method," either of which result in a "gradation sequence signal" as claimed. Ex. 3, ¶¶ [0225]-[0226]; Ex. 19, ¶¶ [0037]- [0039]. Dr. Fontecchio notes that "a POSA would have understood that either method could be used in conjunction with the circuit shown in figure1A", additionally, in its discussion of embodiment 5, Kimura I makes clear that either method could be used with respect to the circuit shown in Fig. 1A. Ex. 3, ¶¶ [0225]-[0226] ("FIG. 24A schematically shows timing of operation and FIG. 24B shows timing of pulses inputted to the first to third gate signal lines in FIG. 1A... When it is driven by an analog gradation method, a period indicated by 2400 is one frame period. When it is driven by a digital time gradation method, the period indicated by 2400 is one sub-frame period."). Thus, Kimura I describes use of the described gradation techniques (i.e., analog gradation or digital

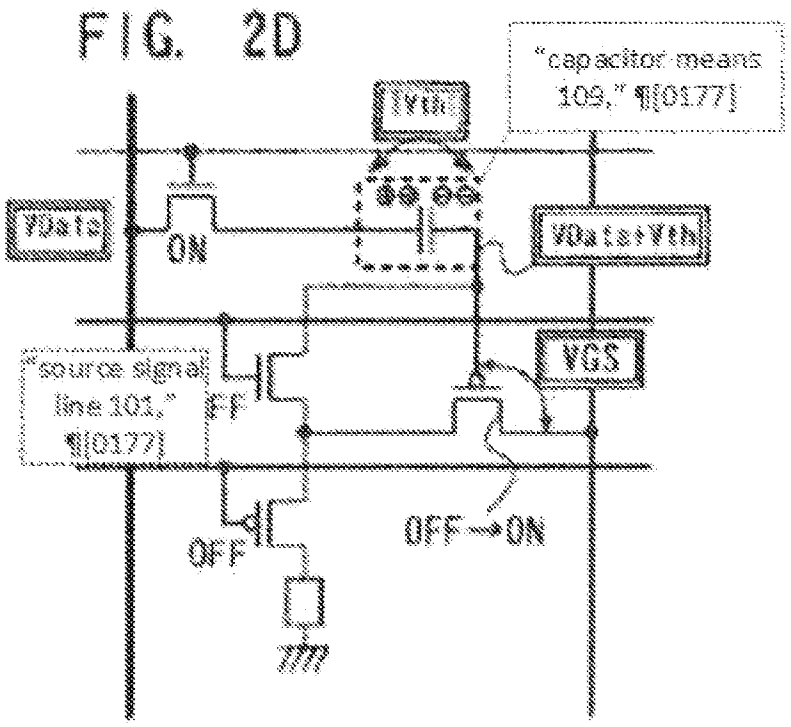
time gradation) to determine the appropriate value of Vdata to supply to the light emission drive circuit. M.P.E.P. § 2143; KSR, 550 U.S. at 415-421.

iii. Kimura I discloses that the electric charge accumulating section "accumulate[es] electric charges based on a gradation sequence signal to designate a luminance gradation sequence in accordance with display data,"

As discussed above, Kimura I discloses an electric charge accumulating section, capacitor means 109, and a gradation sequence signal, Vdata.

Kimura I discloses that capacitor means 109 "accumulate[es] electric charges" based on Vdata "to designate a luminance gradation sequence in accordance with display data," as recited in claim 11. Vdata corresponds to a video signal (i.e., "display data').
Ex. 3, ¶¶ [0182]-[0183] ("The video signal is outputted ... and its potential is changed from VDD to a potential of the video signal Vdata.").

As shown in Fig. 2D of Kimura I, reproduced below, Kimura I discloses the accumulation of electric charges—shown as '+' and '-' symbols—on the capacitor means 109 based on the application of Vdata from the source signal line 101. Ex. 3, ¶ [0183].

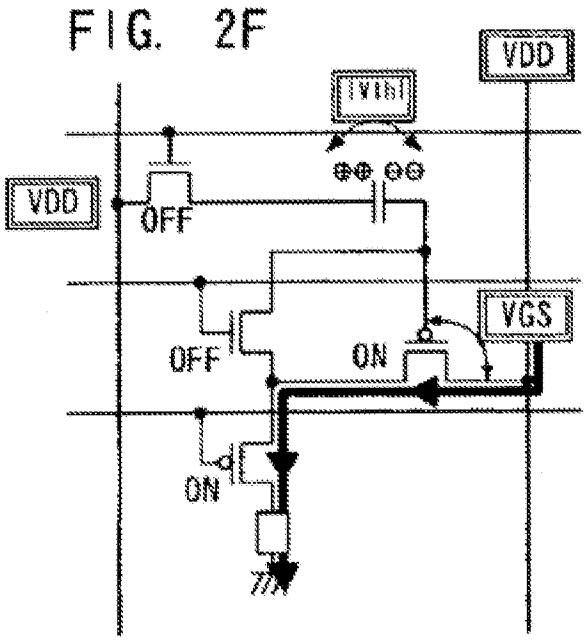


Ex. 3, Fig. 2D (annotated).

The electric charges that accumulate on capacitor means 109, based on Vdata, designate a "luminance gradation [i.e., level] sequence in accordance with display data" by controlling the value of the current (i.e., the luminance level) that flows to the EL element 7110 for light emission. Ex. 3, ¶ [0783] (Thus, a voltage between both electrodes of the capacitor means 109 Is not changed. Accordingly, a potential of the gate electrode of the second TFT 106 become a potential obtained by adding the threshold value Vin to the potential video signal Vdata'), [0185] (At this time, a value of the current flowing into the EL element depends on a voltage between the gate and the source of second TFT 106...Here, even if the threshold value Vth of the second TFT 106 is varied among the second TFTs 106 of respective pixels, a voltage

corresponding to the variation is held in the capacitor means 109 of the respective pixels. Thus, there is no case where the intensity of the EL element 110 is influenced by the variation in the threshold value.").

Fig. 2F depicts the current flowing to the EL element 110 based on the charge accumulated on capacitor means 109:



Ex. 3, Fig. 2F; id., ¶¶ [0183]-[0185].

For at least these reasons, Kimura I teaches this limitation.

With regard to claim 11, further teaches ***(c) a light emission drive circuit having a light emission control section for generating a light emission drive current having***

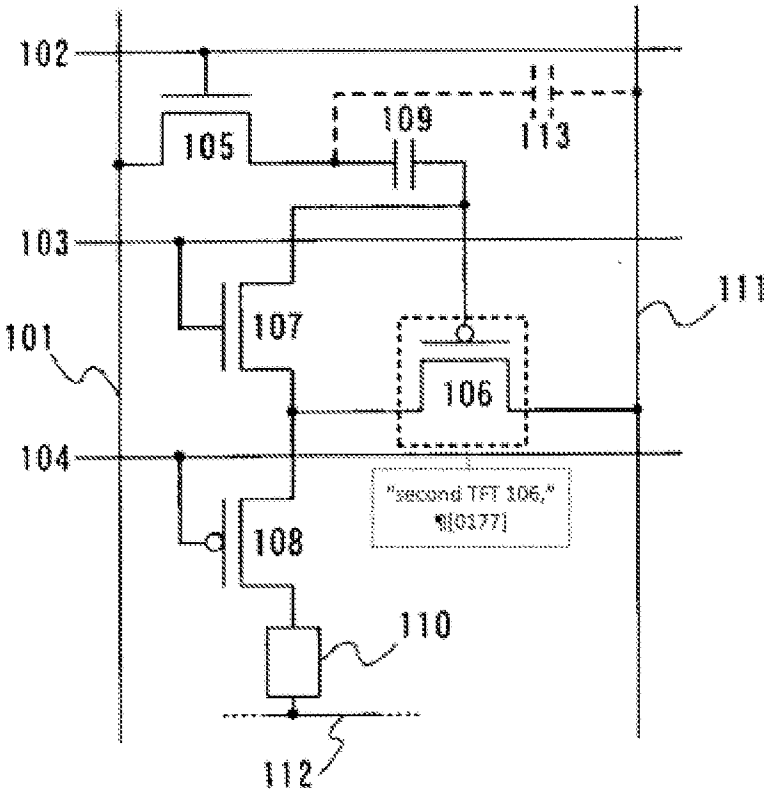
a predetermined current value in accordance with the electric charges accumulated in the electric charge accumulating section and supplying the light emission drive current to the light emission element, Kimura I teaches limitation [11c] as addressed in four parts below.

i. Kimura discloses a "light emission control section" as part of its "light emission drive circuit."

As discussed in Section IX.A.2 of the Request, Patent Owner previously agreed that the term "light emission control section" should be construed as "drive transistor." Kimura I discloses a second TFT 106, which serves as a drive transistor. Ex. 3, ¶ [0185] ("At this time, a value of the current flowing into the EL element depends on a voltage between the gate and the source of second TFT 106").

As shown in Fig. 1A below, second TFT 106 is part of the light emission drive circuit (i.e., elements 105-109):

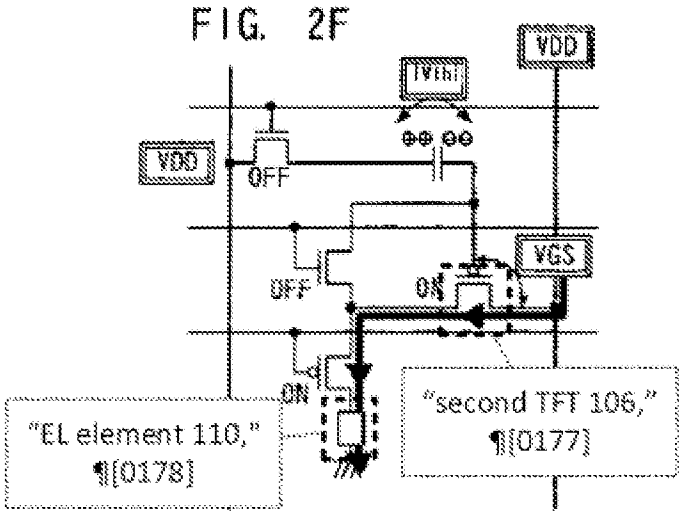
FIG. 1A



Ex. 3, Fig. 1A (annotated).

ii. Kimura I discloses that the light emission control section "generat[es] a light emission drive current"

Referring to Fig. 2F below, Kimura I discloses that second TFT 106 generates a light emission drive current (shown as the thick black arrow) that flows to the EL element 110 for light emission. Ex. 3, ¶¶ [0183]-[0185] ("Accordingly, the second TFT 106 is turned ON (section V)... Thus, as shown in FIG. 2F, a current flows into the EL element so that the EL element emits light"), Fig. 2F.



Ex. 3, Fig. 2F (annotations added).

iii. Kimura I discloses that the light emission drive current has a "predetermined current value in accordance with the electric charges accumulated in the electric charge accumulating section."

Kimura I discloses that the light emission drive current has a predetermined current value in accordance with the electric charges stored on capacitor means 109.

As discussed above with respect to limitation 11[b], charges are accumulated on capacitor means 109 based on the application of Vdata, which corresponds to particular image data. Id., ¶ [0183].

The light emission drive current that flows through the EL element 110 corresponds to the voltage between the gate and source of the light emission control section (i.e., drive

transistor), represented by Vgs in Fig. 2F above. Ex. 3, ¶ [0185] ("At this time, a value of the current flowing into the EL element depends on a voltage between the gate and the source of the second TFT 106.").

Vgs is determined by the electric charges previously accumulated on capacitor means 109 (i.e., the claimed electric charge accumulating section), and thus the light emission drive current is predetermined in accordance with the electric charges. Ex. 3, ¶ [0183] ("Thus, a voltage between both electrodes of the capacitor means 109 is not changed. Accordingly, a potential of the gate electrode of the second TFT 106 become a potential obtained by adding the threshold value Vin to the potential of the video signal Vdata').

iv. Kimura I discloses that the light emission control section "suppl[ies] the light emission drive current to the light emission element."

As shown in Fig. 2F above, Kimura I discloses that the light emission control section, second TFT 106, supplies the light emission drive current to the light emission element, EL element 110, as claimed. Ex. 3, ¶¶ [0183]-[0185] ("Accordingly, the second TFT 106 is turned ON (section V)... Thus, as shown in FIG. 2F, a current flows into the EL element so that the EL element emits light"), Fig. 2F.

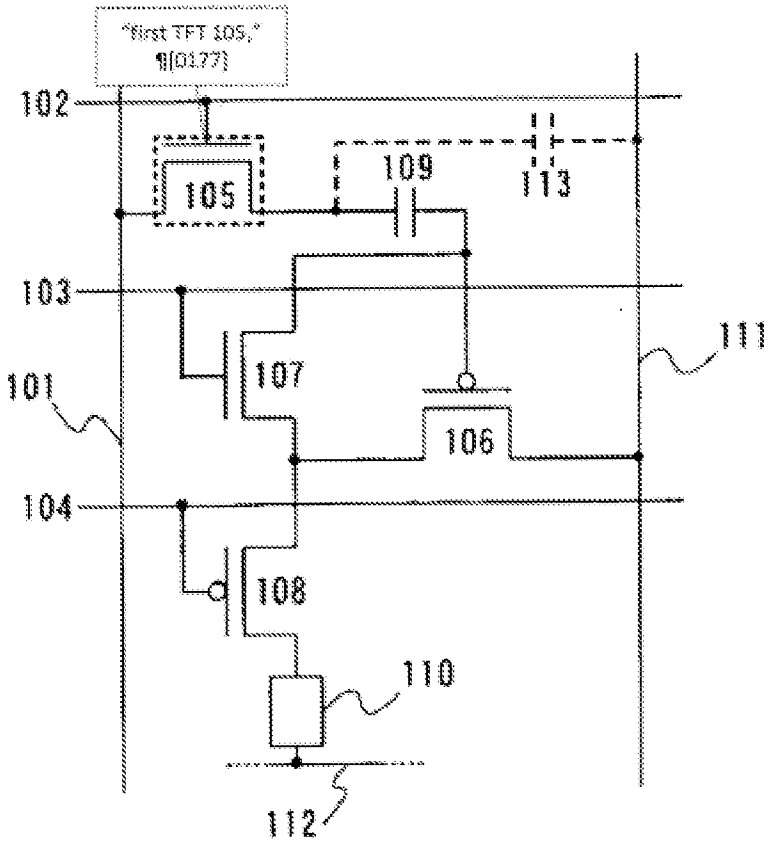
With regard to claim 11, further teaching ***(d) a writing control section for controlling a supplying state of the electric charges based on the gradation sequence signal to the electric charge accumulating section***, Kimura I discloses this limitation. For convenience, limitation [11d] is addressed in two parts below.

i. Kimura I discloses a "writing control section" as part of its "light emission drive circuit."

As discussed in Section IX.A.5 of the Request, Kimura I discloses a "writing control section" under either previously asserted construction.

As shown below in Fig. 1A, Kimura I discloses a "writing control section" (i.e., first TFT 105) included in its light emission drive circuit (i.e., elements 105-109):

FIG. 1A

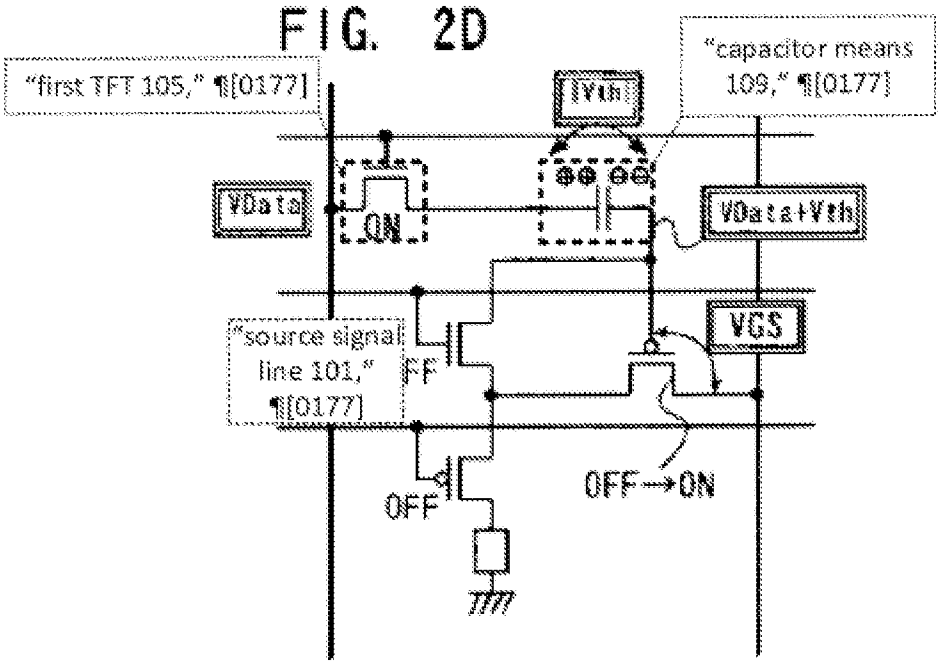


Ex. 3, Fig. 1A (annotated).

First TFT 105 controls the writing of both the gradation sequence signal (Vdata) and the precharge voltage (VDD) from a data line (source signal line 101). Ex. 3, ¶ [0180] ("First, the first gate signal line 102 becomes an H level so that the first TFT 105 is turned ON (section I)."), Fig. 2A (Showing VDD flowing from source signal line 101 through first TFT 105), [0183] ("The video signal is outputted to the source signal line 101 and its potential is changed from VDD to a potential of the video signal Vdata'), [0184] ("Then, when writing of the video signal is completed, as shown in FIG. 2E, the first gate signal line 102 becomes an L level so that the first TFT 105 is turned OFF.").

ii. Kimura I discloses that the writing control section "control[s] a supplying state of the electric charges based on the gradation sequence signal to the electric charge accumulating section."

As discussed above in connection with limitation [11b], Kimura I discloses supplying a gradation sequence signal (Vdata) to the light emission drive circuit by the source signal line 101. Ex. 3, [0183]. As shown in the figure below, the writing control section (first TFT 105) controls the transmission of the signal from the source signal line 101 to the electric charge accumulation section (capacitor means 109) by turning ON and OFF, and thereby supplies a state of electric charge to the charge accumulating section. id., ¶¶ [0180]-[0184].

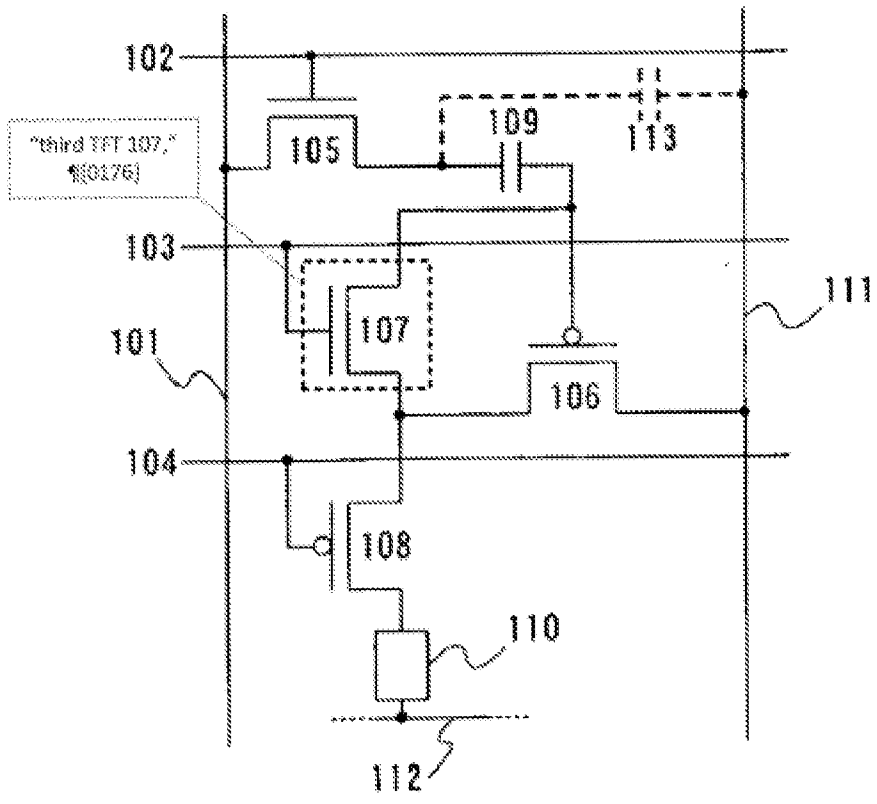


With regard to claim 11 further teaching ***(e) a voltage control section for controlling a drive voltage for making the light emission control section perform the operation, respectively***; Kimura I discloses this limitation. For convenience, limitation [11e] is addressed in two parts below.

i. Kimura I discloses a "voltage control section" as part of its "light emission drive circuit."

As shown below in Fig. 1A, Kimura I discloses a "voltage control section" (i.e., third TFT 107) included in its light emission drive circuit (i.e., elements 105-109):

FIG. 1A



Ex. 3, Fig. 1A (annotations added); see also id., ¶ [0176].

ii. Kimura I discloses that its voltage control section "control[s] a drive voltage for making the light emission control section perform the operation."

Patent Owner previously argued that "the operation" refers to "generating a light emission drive current having a predetermined current value in accordance with the electric charges accumulated in the electric charge accumulating section and supplying the light emission drive current to the light emission element." (see Section IX.A.3 of the Request)

As discussed in Section IX.A.3 of the Request, Requester submits that the broadest reasonable interpretation of "the operation" should include the above functionality. Third TFT 107 is used to "control[] a drive voltage for making the light emission control section perform the operation," as claimed.

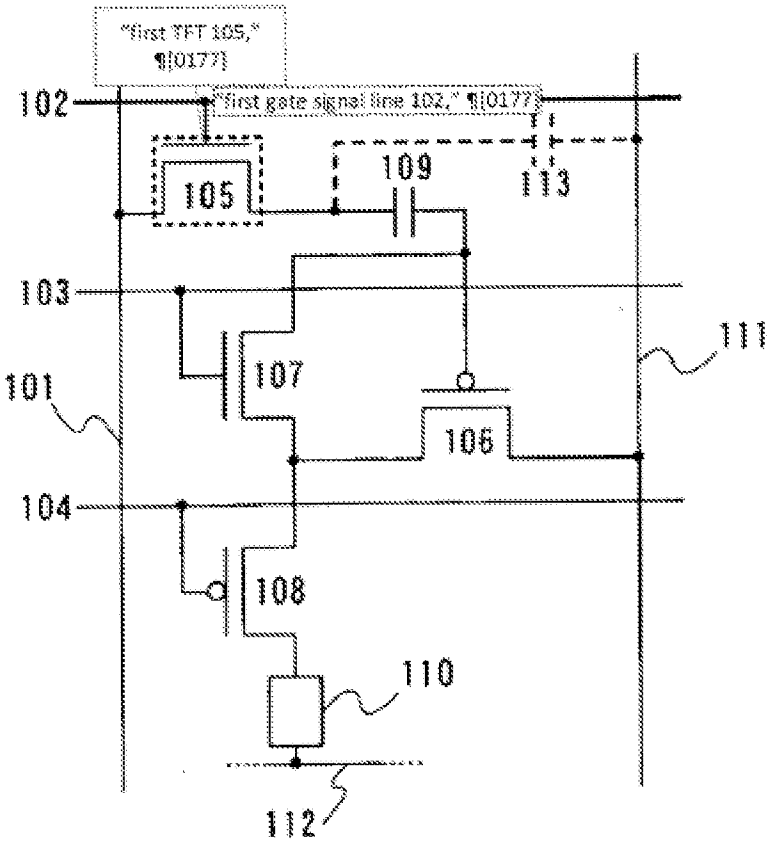
As discussed above in connection with limitation [11c], the light emission control section (second TFT 106) performs the "operation," by supplying a light emission drive current to the light emission element. Ex. 3, [0185] ("Thus, as shown in FIG. 2F, a current flows into the EL element so that the EL element emits light').

Third TFT 107 controls the value of the voltage being held by capacitor means 109 (i.e., the claimed "electric charge accumulation section") on the gate of the second TFT 106 (i.e., the "light emission control section"), and thereby controls its "drive voltage" as

claimed. Ex. 3, ¶ [0180] ("Subsequently, the second gate signal line 103 becomes an H level... so that the third TFT 107.... [is] turned ON (section II). Here, as shown in FIG. 2A, the capacitor means 109 is charged"), Ex. 3, ¶ [0182] ("After that, the second gate signal line 103 becomes an L level so that the third TFT 107 is turned OFF (section IV). By such operation, as shown in FIG. 2C, Vin is held in the capacitor means 109.").

With regard to claim 11, further teaching ***(f) selection lines in which writing control signals for controlling the operation state of the writing control sections of the display pixels are applied***; Kimura I discloses a first signal gate line 102 (i.e., a "selection line") that is connected to the gate of a first TFT 105 (i.e., the claimed "writing control section"). Ex. 3, ¶¶ [0176]-[0178].

FIG. 1A



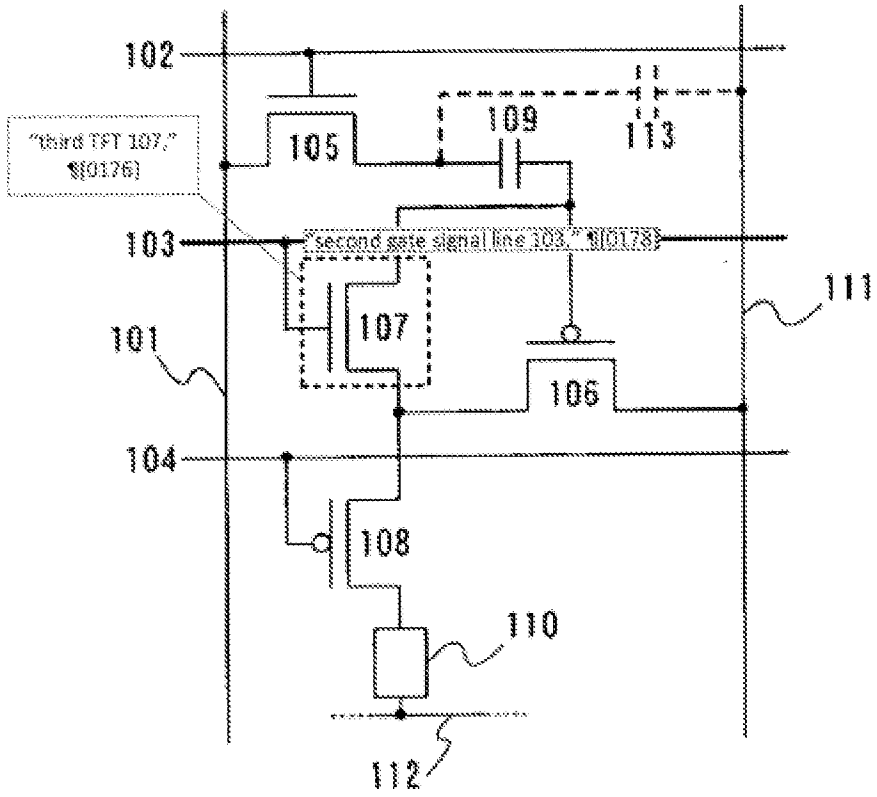
Kimura I, Fig. 1A (annotations added). Kimura I discloses that its displays will have a matrix of the pixels shown above. Ex. 3, ¶ [0193] ("The device has a pixel portion 702 wherein a plurality of pixels is arranged in a matrix shape"). Accordingly, a plurality of selection lines would be used. one for each row of pixels. Id., ¶ [0200] ('the first gate signal line driver circuit sequentially selects first gate signal lines Gi1, Ga1,...and Gm").

The first gate signal lines 102 (i.e., "selection lines") "control[] the operational state of the writing control section" (i.e., first TFT 105) using "writing control signals

(i.e., "H level" and "L level"). Ex. 3, ¶¶ [0180] ("First, the first gate signal line 102 becomes an H level so that the first TFT 105 is turned ON"), [0184] ("Then, when writing of the video signal is completed, as shown in FIG. 2E, the first gate signal line 102 becomes an L level so that the first TFT 105 is turned OFF"); see also id., ¶ [0193] ("In FIG. 7A, three gate signal line driver circuits are used, which control first to third gate signal lines of pixels shown in FIG. 1.").

With regard to claim 11, further teaching ***(g)*** **hold lines in which voltage control signals for controlling the operation state of the voltage control sections of the display pixels are applied**; Referring to Fig. 1A below, Kimura I discloses a second gate signal line 103 (i.e., a "hold line") that is connected to the gate of a third TFT 107 (i.e., the claimed "voltage control section"). Ex. 3, ¶¶ [0176]-[0178].

FIG. 1A



Ex. 3, Fig. 1A (annotations added). Kimura I discloses that its displays will have a matrix of pixels as shown above. Id., ¶ [0193] ("The device has a pixel portion 702 wherein a plurality of pixels is arranged in a matrix shape"). Accordingly, a plurality of hold lines would be used, one for each row of pixels. Id., ¶ [0200] ("the second gate signal line driver circuit sequentially selects second gate signal lines G21, G22,...and Gm").

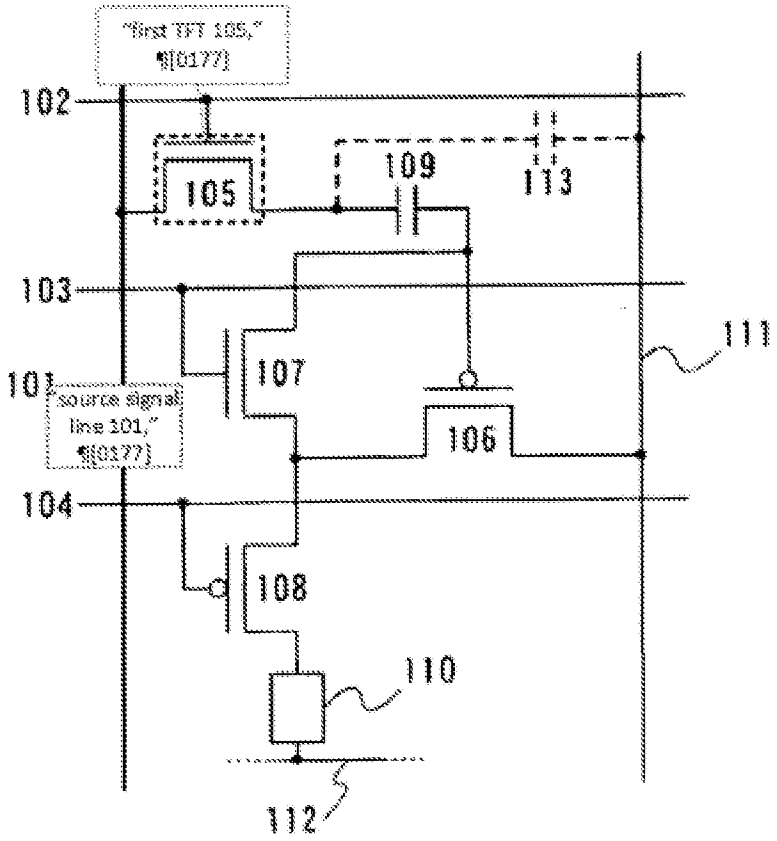
The second gate signal lines 103 (i.e., "hold lines") "control[] the operation state of the voltage control section" (i.e., third TFT 107) using "voltage control signals" (i.e., "H level" and "L level"). Ex. 3, ¶ [0180] ("Subsequently. the second gate signal line 103 becomes an H level... so that the third TFT 107... [is] turned ON."); id., ¶ [0182] ("After that, the

second gate signal line 103 becomes an L level so that the third TFT 107 is turned OFF"); see also id., ¶ [0193] ("In FIG. 7A, three gate signal line driver circuits are used, which control first to third gate signal lines of pixels shown in FIG. 1.").

With regard to claim 11, further teaching ***(h)* data lines to which the gradation sequence signals are supplied**; As discussed in Section IX.A.6 of the Request, Kimura I discloses "data lines" under either previously asserted construction.

Referring to Fig. 1A below, Kimura I discloses a source signal line 101 (i.e., a "data line") connected to the first electrode of the first TFT 105. Ex. 3, ¶¶ [0176]—[0178].

FIG. 1A



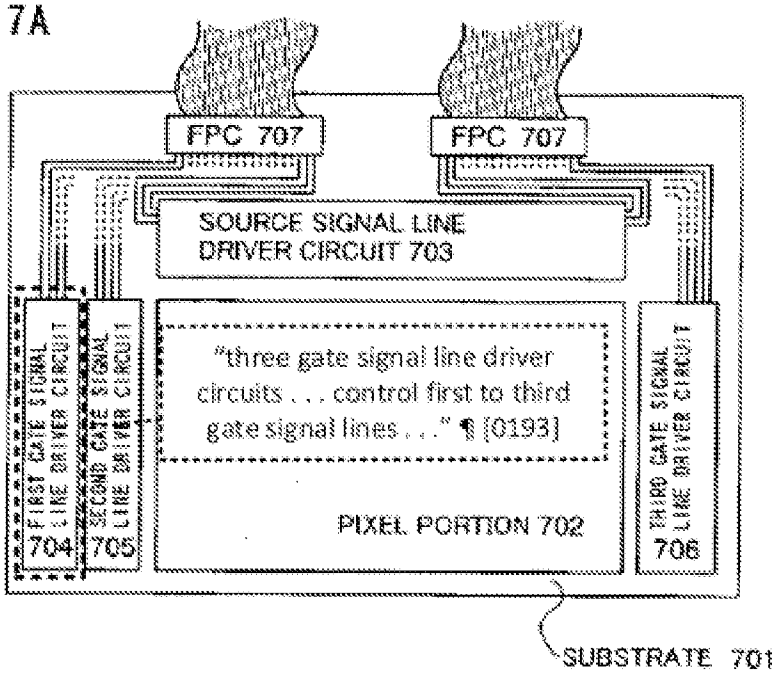
Ex. 3, Fig. 1A (annotations added).

The source signal line 101 is a conductive line. It conveys electrical signals corresponding to video signals to the pixel light emission drive circuit. Ex. 3, ¶¶ [0180]-[0184], [0198] ("The potential held by the video signals at this time is outputted to the respective source signal lines."). Kimura I discloses that its displays will have a matrix of the pixels shown above. Ex. 3, ¶ [0193] ("The device has a pixel portion 702 wherein a plurality of pixels is arranged in a matrix shape"). Accordingly, a plurality of data lines would be used, one for each column of pixels. The source signal lines 101 ("data lines") further supply a "gradation sequence signal" in the form of Vdata to the

writing control sections (first TFT 105) of the various pixels. See Ex. 3, ¶¶ [(0180]-[0184], [0198] ("The potential held by the video signals at this time is outputted to the respective source signal lines.").

With regard to claim 11, further teaching ***(i)* a selection driver which applies the writing control signals in the selection lines**; Kimura I discloses "a selection driver' (i.e., first gate signal line driver circuit 704):

FIG. 7A



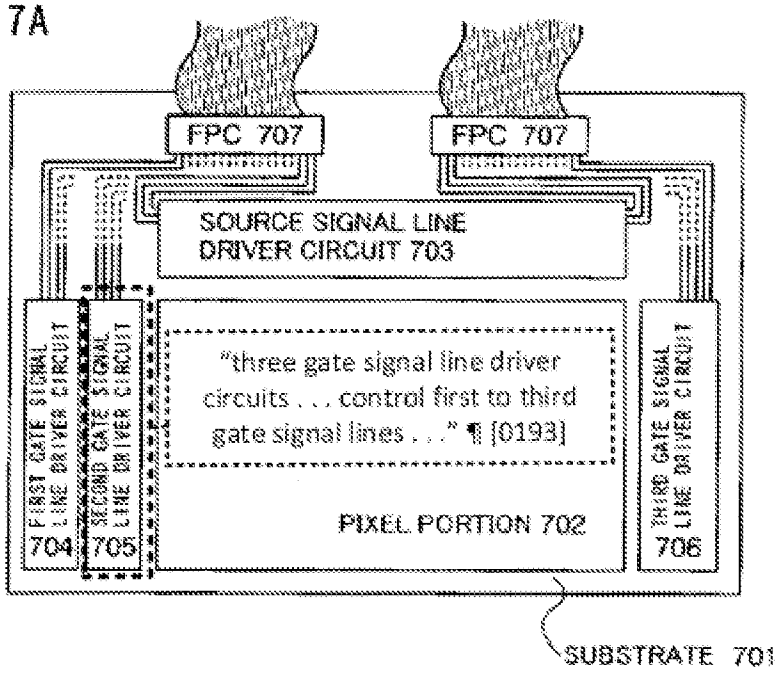
Ex. 3, Fig. 7A (annotated).

More generally, Kimura I discloses "first to third gate signal line driver circuits 704 and 706" and that "[i]n FIG. 7A, three gate signal line driver circuits are used, which

control first to third gate signal lines of pixels shown in FIG. 1." Ex. 3, ¶ [0193]. The first to third gate signal lines are signal lines 102-104. Id., ¶ [0193]. Accordingly, the "selection driver" (i.e., first gate signal line driver circuit 704) is associated with the first gate signal line 102 of Kimura I, and "applies the writing control signals" in the first gate signal lines 102 (i.e., the claimed "selection lines"). Id., ¶¶ [0180] ("the first gate signal line 102 becomes an H level so that first TFT 105 is turned ON"), [0193] ("three gate signal line driver circuits are used, which control first to third gate signal lines of pixels shown in FIG. 1."), [0200] ("the first gate signal line driver circuit sequentially selects first gate signal lines G11, G21,...and Gm1").

With regard to claim 11, further teaching ***(j)*** **a hold driver which applies the voltage control signals in the hold lines**; Kimura I discloses "a hold driver" (i.e., second gate signal line driver circuit 705):

FIG. 7A

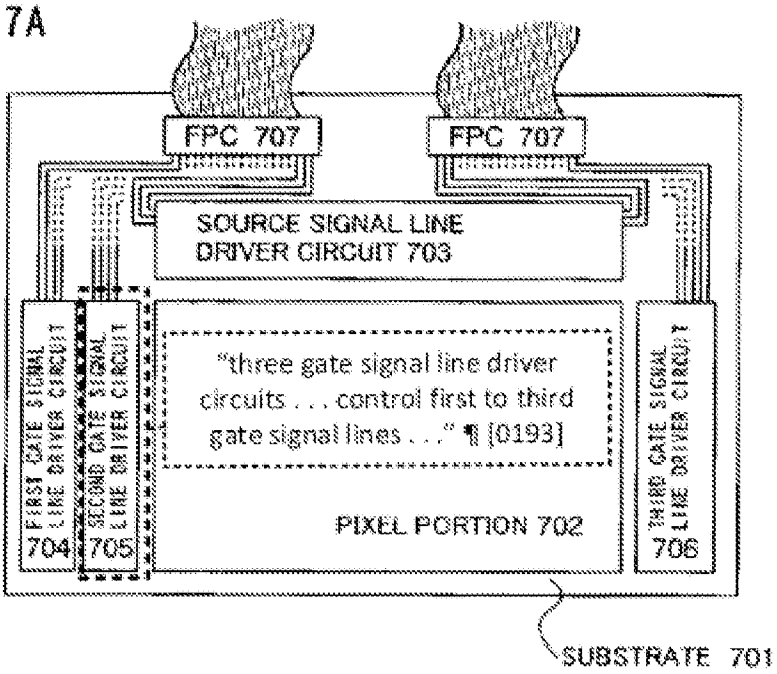


Ex. 3, Fig. 7A (annotated).

More generally, Kimura I discloses "first to third gate signal line driver circuits 704 and 706" and that "[i]n FIG. 7A, three gate signal line driver circuits are used, which control first to third gate signal lines of pixels shown in FIG. 1." Ex. 3, ¶ [0193]. The first to third gate signal lines are signal lines 102-104. Id. Accordingly, the "hold driver" (i.e., second gate signal line driver circuit 705) is associated with the second gate signal line 103 of Kimura I, and "applies the voltage control signals" in the second gate signal lines (i.e., the claimed "hold lines'). Id., ¶¶ [0180] ("second gate signal line 103 becomes an H level... so that third TFT 107... [is] turned ON"), [0193] ("three gate signal line driver circuits are used, which control first to third gate signal lines of pixels shown in FIG. 1."). [02001 ("the second gate signal line driver circuit sequentially selects second gate signal lines G12, G22,...and Gm2").

With regard to claim 11, further teaching ***(k)* a data driver which supplies the gradation sequence signals to the data lines**; Kimura I discloses "a hold driver" (i.e., second gate signal line driver circuit 705):

FIG. 7A



Ex. 3, Fig. 7A (annotated).

More generally, Kimura I discloses "first to third gate signal line driver circuits 704 and 706" and that "[i]n FIG. 7A, three gate signal line driver circuits are used, which control first to third gate signal lines of pixels shown in FIG. 1." Ex. 3, ¶ [0193]. The first to third gate signal lines are signal lines 102-104. Id. Accordingly, the "hold driver" (i.e., second gate signal line driver circuit 705) is associated with the second gate signal line 103 of Kimura I, and "applies the voltage control signals" in the second gate signal lines (i.e., the claimed "hold lines'). Id., ¶¶ [0180] ("second gate signal line 103 becomes an

H level... so that third TFT 107... [is] turned ON"), [0193] ("three gate signal line driver circuits are used, which control first to third gate signal lines of pixels shown in FIG. 1."), [0200] ("the second gate signal line driver circuit sequentially selects second gate signal lines G12, G22,...and Gm2").

With regard to claim 11, further teaching ***(l)*** **wherein, with respect to each of the display pixels, the data driver applies a precharge voltage exceeding a threshold value of the drive transistor to the data line, and the light emission drive circuit applies the precharge voltage applied to the data line to the electric charge accumulating section via the writing control section,**

Limitation [11l] is addressed in three parts below.

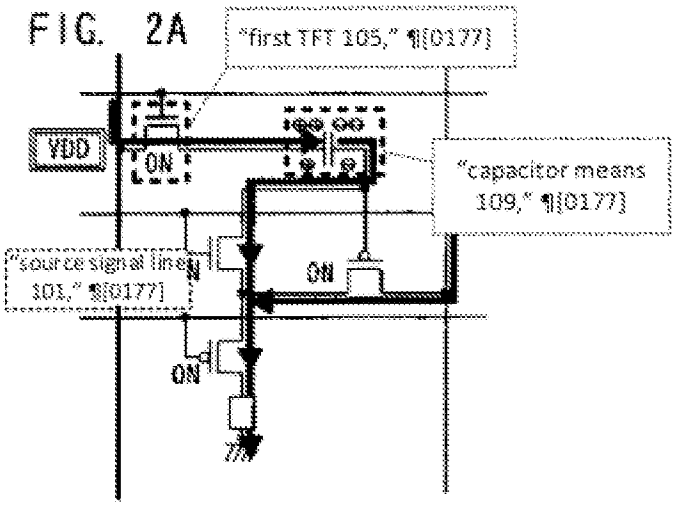
Note: the '615 Patent specification refers to two separate 'precharge voltages' (see column 19 line 33 through column 20, line 67):

(1) the precharge voltage applied to the data line;

(2) the precharge voltage measured between the opposite ends of the electric charge accumulation section that exceeds a threshold value of the drive transistor.

<u>i. Kimura I discloses that the "data driver applies a precharge voltage... to the data line."</u>

First, Kimura I discloses the "data driver applies a precharge voltage . . . to the data line." As discussed above, Kimura I discloses a source signal line driver circuit (i.e., the claimed "data driver") that applies a signal VDD (i.e., the claimed "precharge voltage") to the source signal lines (i.e., the claimed "data lines"). See limitation [11k], above; see also Ex. 3, ¶¶ [0193]-[0198]:



Ex. 3, Fig. 2A (annotations added)

The voltage VDD provided by the source signal line driver circuit is the claimed "precharge voltage." It is applied to the data line before the gradation sequence signal (i.e., Vdata voltage). See Ex. 3, ¶¶ [0183] ("The video signal is outputted to the source signal line 101 and its potential is changed from VDD to a potential of the video signal Vdata'), [0184] ("After that, the output of the video signal to the source signal line is also completed and its potential is returned to VDD."); see also id., ¶¶ [0179]-[0186], Figs. 2A-2F.

ii. Kimura I discloses that the precharge voltage "exceeds the threshold value of the drive transistor."

Second, Kimura I discloses that the precharge voltage applied to the data line, i.e., VDD, "exceeds the threshold value of the drive transistor" (the claimed light emission control section), second TFT 106.

In particular, Kimura I discloses that the voltage held across capacitor means 109 exceeds the threshold value of the drive transistor. Ex. 3, ¶ [0180] ("[A]ls shown in FIG. 2A, the capacitor means 109 is charged, and when a voltage held by the capacitor means 109 exceeds a threshold value (Vth) of the second TFT 106, the second TFT 106 is turned on.") (emphasis added).

As shown in FIG. 2A, during "section II" of the timing diagram (see FIG 1B), third TFT 107 and fourth TFT 108 are turned on, and the right plate of the capacitor is connected to ground through the EL element 110. Ex. 3, ¶ [0180]. Thus, the voltage across the capacitor is equal to VDD (i.e., the voltage measured on the left plate of the capacitor) minus the voltage drop associated with EL element 110 (i.e., the voltage measured on the right plate of the capacitor).

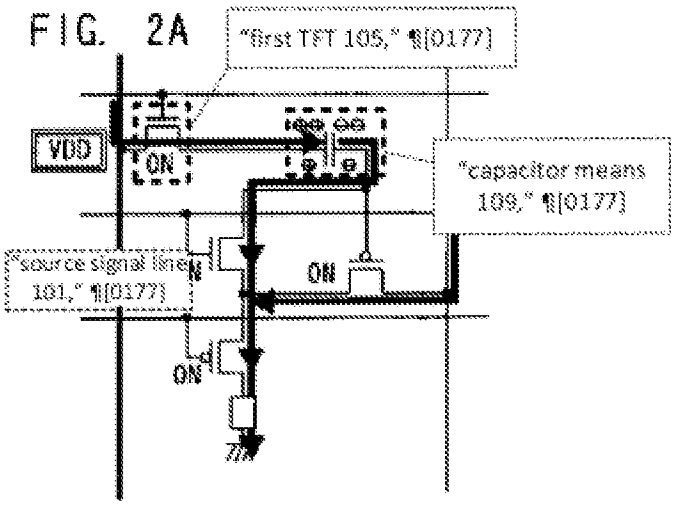
Given that the voltage across the capacitor exceeds the threshold voltage of the drive transistor, and that the voltage across the capacitor is equal to VDD minus the

voltage across the EL element, Von (the "precharge voltage") must also exceed the "threshold value of the drive transistor [second TFT 106]," as claimed.

iii. Kimura I discloses that the light emission drive circuit "applies the precharge voltage applied to the data line to the electric charge accumulating section via the writing control section."

Kimura I discloses that the light emission drive circuit (i.e., elements 105-109) "applies the precharge voltage applied to the data line," (i.e., VDD), "to the electric charge accumulating section" (i.e., capacitor means 109), "via the writing control section" (i.e., first TFT 105). See Ex. 3, ¶ [0180] ("First, the first gate signal line 102 becomes an H level so that the first TFT 105 is turned ON (section I)... Here, as shown in FIG. 2A, the capacitor means 109 is charged, and when a voltage held by the capacitor means 109 exceeds a threshold value (Vin) of the second TFT 106, the second TFT 106 is turned ON.").

As shown in Fig. 2A, below, VDD is applied to the capacitor means 109 via the first TFT 105:

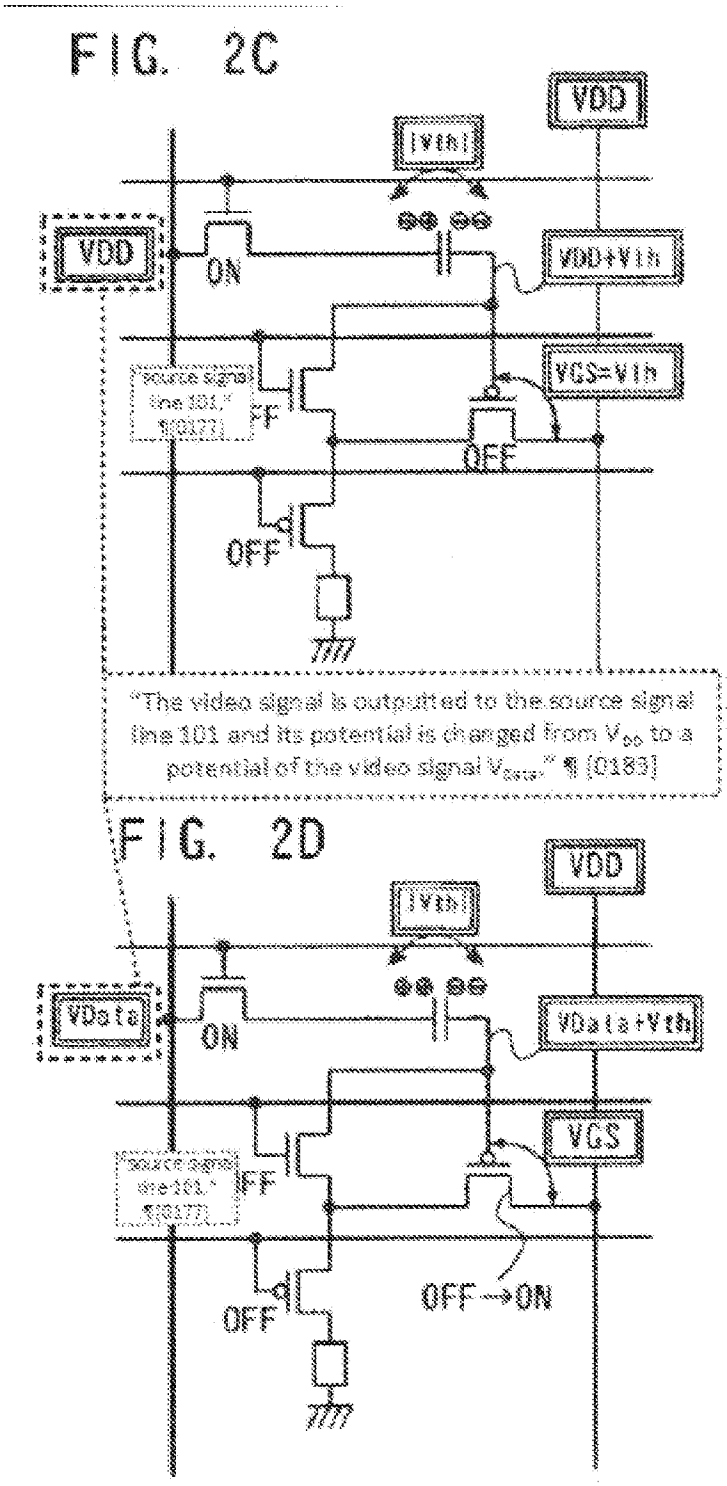


With regard to claim 12, further teaching ***wherein the light emission drive circuit partially discharges the electric charges accumulated in the electric charge accumulating section on the basis of the precharge voltage and maintains the electric charges equivalent to the threshold voltage of the drive transistor,*** Kimura I also discloses "wherein the light emission drive circuit partially discharges the electric charges accumulated in the electric charge accumulating section on the basis of the precharge voltage and maintains the electric charges equivalent to the threshold voltage of the drive transistor," as claimed. See Ex. 3, ¶ [0181] ("Subsequently, as shown in FIG. 2B, the third gate signal line 104 becomes an H level so that the fourth TFT 108 is turned OFF. Then, charges stored in the capacitor means 109 move again, and soon a voltage held by the capacitor means 109 becomes equal to Vth....")

With regard to claim 13, further teaching ***wherein the precharge voltage and the gradation sequence signal applied from the data driver to the data line are applied in the electric charge accumulating section via the writing control section at different timings, respectively,*** As discussed above in connection with limitation [11], Kimura I discloses a "precharge voltage" (i.e., VDD in Kimura I) that is supplied from the "data driver to the data line" and is "applied to the electric charge accumulating section via the writing control section."

As discussed above in connection with limitation [11d], Kimura I discloses a "gradation sequence signal" (i.e., Vdata in Kimura I) that is supplied from the "data driver to the data line" and is "applied to the electric charge accumulating section via the writing control section."

Kimura I discloses that the precharge voltage, VDD, and the gradation sequence signal, Vdata, are applied at "different timings, respectively":



Ex. 3, Figs. 2B, 2D (annotations added); see also id., ¶¶ [0182]-[0183] ("Subsequently, as shown in FIG. 2D, a Video signal is inputted (Section V) . . . The video signal

is outputted to the source signal line 101 and its potential is changed from VDD to a potential of the video signal Vdata,"); see also id. [0184] ("After that, the output of the video signal to the source signal line is also completed and its potential is returned to VDD (section VII)." (emphasis added)), Figs. 2A-2F, Fig. 1B.

B. Kimura II

Claims 11 and 13 are rejected under pre-AIA 35 U.S.C. 102 (b) as anticipated by or, in the alternative, under pre-AIA 35 U.S.C. 103(a) as obvious over Kimura II (Ex. 14), U.S. Publication No.: 2004/0227749 (hereinafter Kimura II), as presented on pages 30-35 and 73-115 of the Request and reproduced in part below.

With regard to claim 11, teaching (pre) **A display unit;** Kimura II discloses a plurality of devices, each of which includes a "display unit." Ex. 14, ¶¶ [0288]-[0296], Fig. 36 (noting the "invention can be applied to an electronic circuit configuring the display portion" elements 13003, 13102, 13203, 13302, 13403, 13502, 13602, 13703).

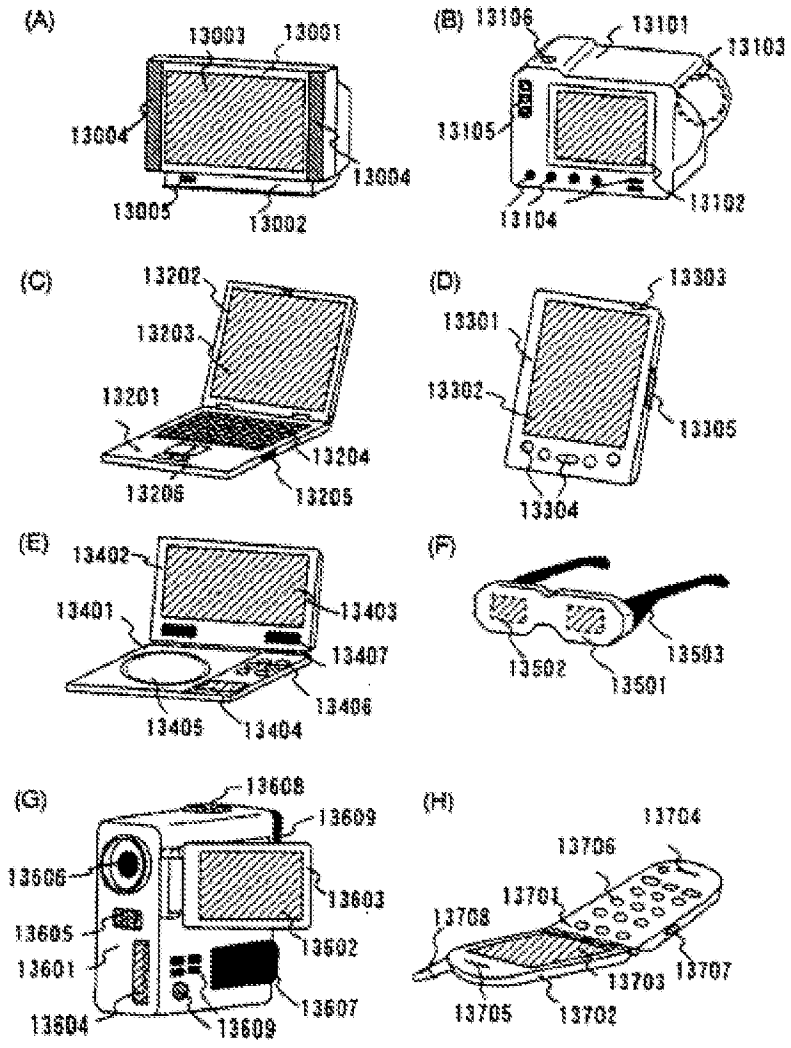
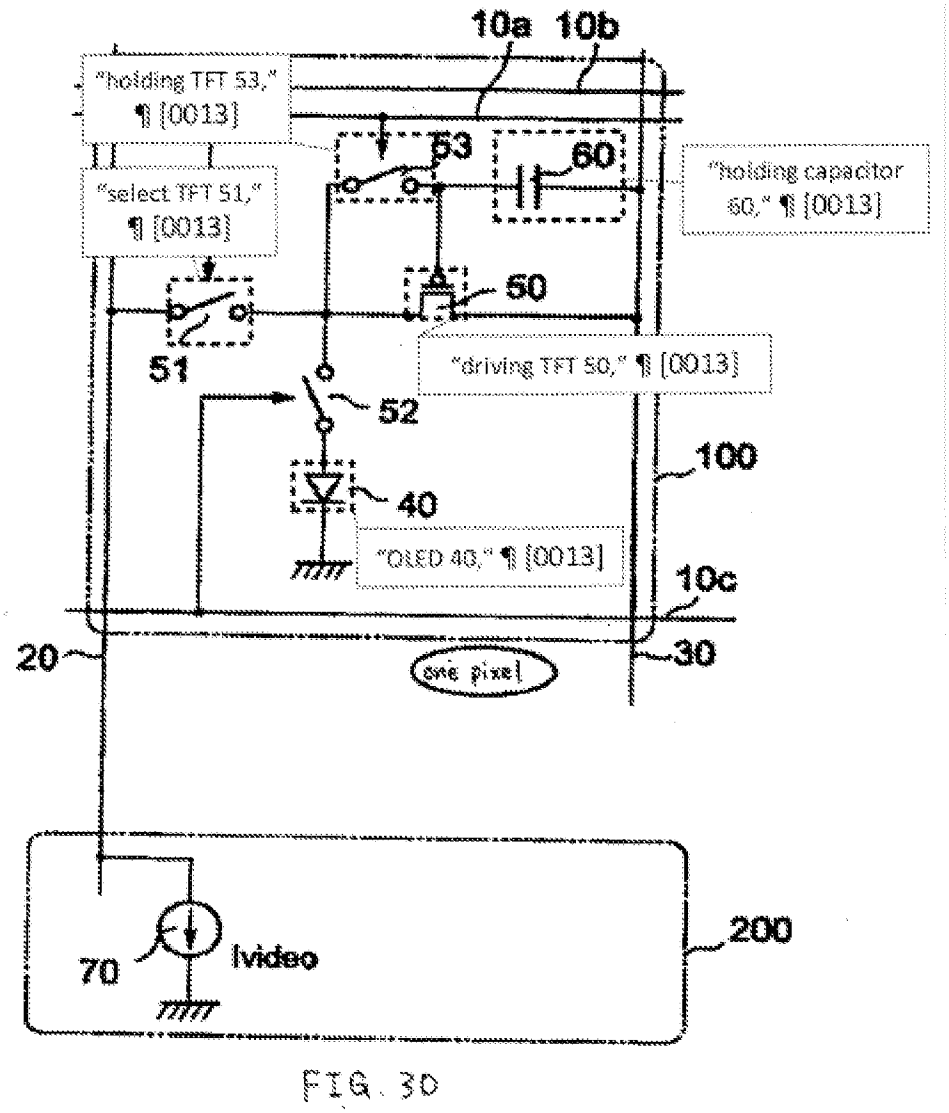


FIG. 36

With regard to claim 11 teaching ***(a) the display unit comprising: a plurality of display pixels each of which includes a light emission element and a light emission drive circuit***, First, Kimura II discloses "a plurality of display pixels." Ex. 14, ¶¶ [(0011]-[0012] ("FIG. 30 is a circuit diagram showing an example of a conventional active matrix display device .. . This display device is configured with a plurality of pixel circuits.").

Furthermore, Kimura ¶¶ discloses that each of the display pixels include "a light emission element and a light emission drive circuit":



Ex. 14, Fig. 30 (annotations added).

Referring to the annotations in Fig. 30 above, Kimura discloses that each of the plurality of pixels includes an OLED 40 that emits light (i.e., a "light emission element'). Ex. 14, ¶ [0012].

Still referring to the annotations in Fig. 30 above, Kimura II discloses each pixel includes "a light emission drive circuit'? that includes light emitting TFT 52. Select TFT 51, driving TFT 50, holding capacitor 60, and holding TFT 53:

The pixel circuit 100 comprises an OLED 40 which is a current drive light emitting element, a light emitting TFT 52 which switches between ON and OFF corresponding to a control signal of a control line 10c, a select TFT 51 which switches between ON and OFF corresponding to a control Voltage of a control line 10b so that a signal current having a current level corresponding to image data supplied to the signal line flows, a driving TFT 50 which supplies driving current from the power supply line 30, a holding capacitor 60 which is connected between the gate and source of the driving TFT 50, a holding TFT 53 which switches between ON and OFF corresponding to a control signal of the control line 10a and selectively connects the gate and drain of the driving TFT 50.

Ex. 14, ¶ [0013]. Kimura II discloses a "light emission drive circuit"

As shown in annotated Fig. 30 above, the light emission drive circuit is connected to the light emitting element 40, as well as a signal line 20, control lines 10a — 10c and power supply line 30. Id. For at least these reasons, Kimura II discloses this limitation.

With regard to claim 11, ***further teaches (b) the light emission drive circuit having an electric charge accumulating section for accumulating electric charges based on a gradation sequence signal to designate a luminance gradation sequence in accordance with display data***, Kimura II discloses this limitation. For convenience, limitation [11b] is addressed in three parts below.

i. Kimura II discloses an "electric charge accumulating section" as part of its "light emission driver circuit."

As discussed in Section IX.A.7 of the Request, Requester submits that the broadest reasonable interpretation of the term "electric charge accumulating section" should include a capacitor. Kimura II discloses an "electric charge accumulating section" (i.e., holding capacitor 60) included in its light emission drive circuit (i.e., elements 50-53, 60):

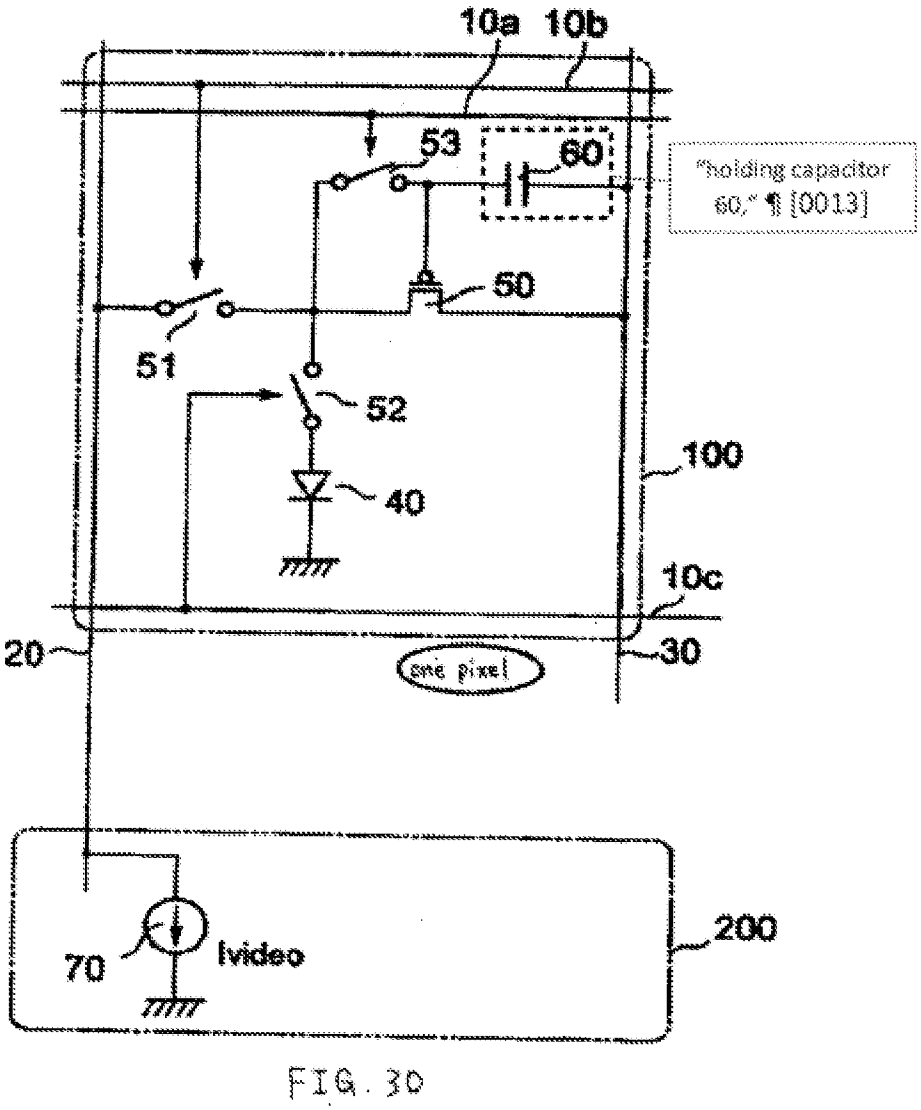


FIG. 30

Ex. 14, Fig. 30 (annotations added). Ex. 14, ¶ [0013] ("The pixel circuit 100 comprises . . . a holding capacitor 60.").

ii. Kimura II discloses a "gradation sequence signal."

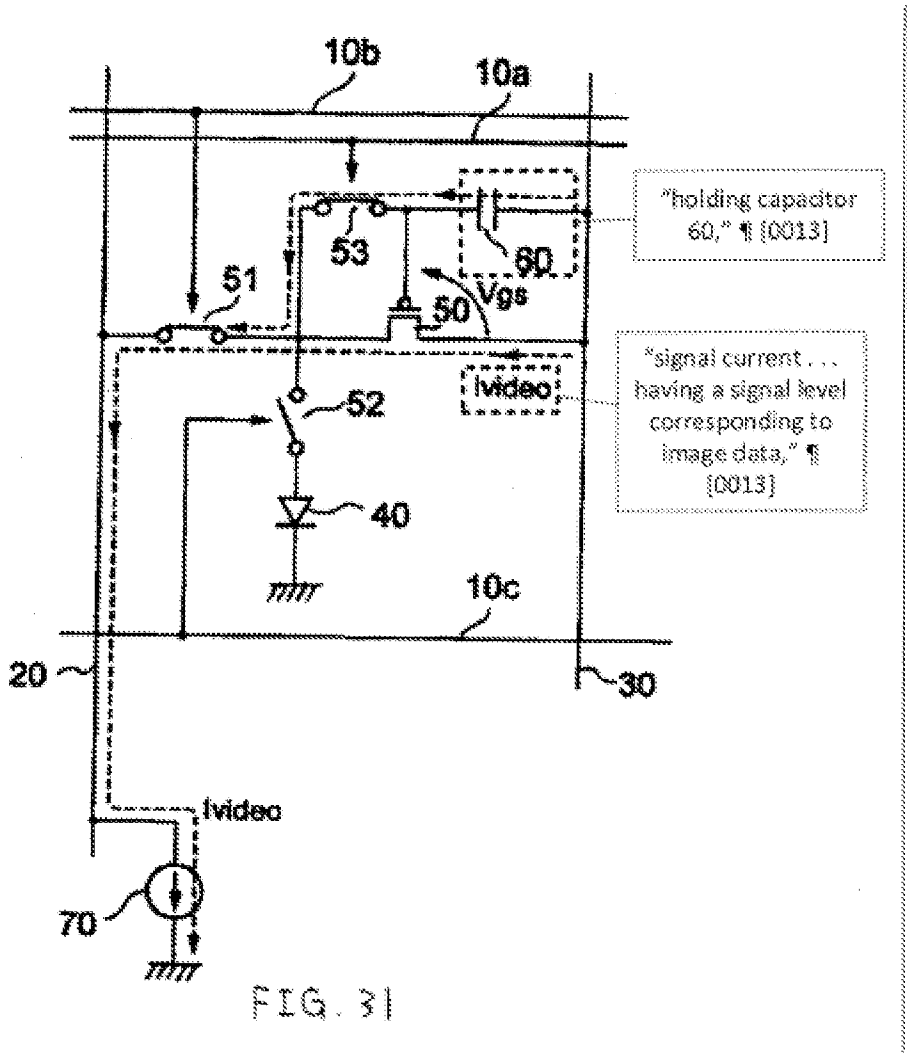
As discussed in Section IX.A.1, Patent Owner previously agreed that the term "gradation" should be construed as "level."

Kimura II discloses a sequence signal level corresponding to a video signal, Ivideo,. Ex. 14, J [0013] (noting that "signal current Ivideo" is a "signal level corresponding to image data"); see also id., ¶ [0015] ("signal current Ivideo . . . is determined by the image signal input current source 70").

iii. Kimura II discloses that the electric charge accumulating section "accumulate[es] electric charges based on a gradation sequence signal to designate a luminance gradation sequence in accordance with display data,"

As discussed above, Kimura II discloses an electric charge accumulating section, holding capacitor 60, and a gradation sequence signal, Ivideo.

Kimura II discloses that holding capacitor 60 "accumulat[es] electric charges" based on the signal current Ivideo "to designate a luminance gradation sequence in accordance with display data" as recited in claim 11. See Fig 14. Fig. 31. reproduced and annotated below:



Ex. 14, Fig. 31 (annotations added).

Referring to Fig. 31 above, Kimura II discloses that signal current Ivideo is applied along the current path denoted by dashed lines. Ex. 14, J [0015]. As shown in Fig. 31, the current path includes the electric charge accumulating section (i.e., Kimura's "holding capacitor 60"). Id. (noting that the application of "signal current Ivideo" results in a voltage, Vgs, that is "stored in the holding capacitor 60."). The voltage across a capacitor is linked to the amount of charge accumulated on the capacitor, through the

well understood equation Q=CV, where Q is the total charge, C is the capacitance value of the capacitor, and V is the voltage across the capacitor. Ex. 19, ¶ [0019].

Ivideo Corresponds to display data. See Ex. 14, ¶ [0013] (noting that "Ivideo" has a "signal level corresponding to image data"), ¶ [0015] (noting that "Ivideo" is determined by "image signal input current source 70").

The electric charges that accumulate on holding capacitor 60 based on Ivideo designate a "luminance gradation [i.e., level] sequence in accordance with display data" by controlling the value of the current (i.e., the luminance level) that flows to the OLED 40 for light emission. Ex. 14, ¶ [0018] ("Then the voltage between the gate and source, Vgs is stored in the holding capacitor 60 and this storage voltage Vgs keeps the signal current Ivideo, flowing to the driving TFT 50... Thus, the signal current Ivideo starts flowing to the OLED 40.")

With regard to claim 11, ***further teaches (c) the light emission drive circuit having a predetermined current value in accordance with the electric charges accumulated in the electric charge accumulating section and supplying the light emission drive current to the light emission element***,

i. Kimura II discloses a "light emission control section" as part of its "light emission drive circuit."

As discussed in Section IX.A.2 of the Request, Patent Owner previously agreed that the term "light emission control section" should be construed as "drive transistor."

Kimura II discloses driving TFT 50. Ex. 14, ¶ [0013] ('The pixel circuit 100 comprises . . . a driving TFT 50."); see also id., ¶ [0018] ("Then the voltage between the gate and source, Vgs is stored in the holding capacitor 60 and this storage voltage Vgs keeps the signal current Ivideo, flowing to the driving TFT 50... Thus, the signal current Ivideo Starts flowing to the OLED 40."). As shown in Fig. 30 below, driving TFT 50 is part of the light emission drive circuit (i.e., elements 50-53, 60):

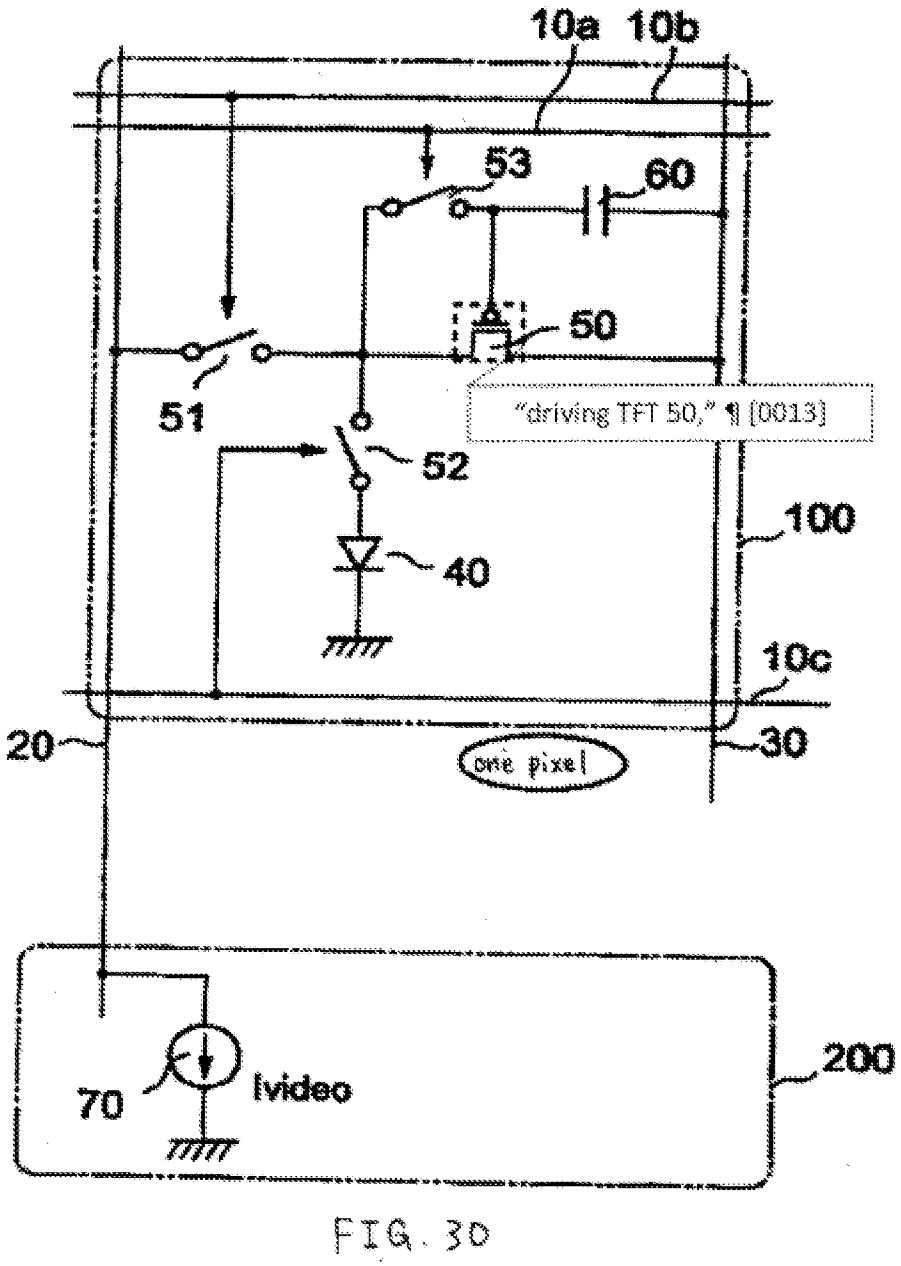


FIG. 30

Ex. 14, Fig. 30 (annotations added).

ii. Kimura II discloses that the light emission control section generates a "light emission drive current."

Kimura II discloses that the light emission control section (driving TFT 50) generates a light emission drive current that flows to OLED 40 for light emission. Ex. 14, ¶ [0018] ("Then the voltage between the gate and source, Vgs is stored in the holding capacitor 60 and this storage voltage Vgs keeps the signal current Ivideo, flowing to the driving TFT 50. . . Thus, the signal current Ivideo Starts flowing to the OLED 40.").

iii. Kimura II discloses that the light emission drive current has a "predetermined current value in accordance with the electric charges accumulated in the electric charge accumulating section."

Kimura II discloses that the light emission drive current has a predetermined current value in accordance with the electric charges stored on holding capacitor 60).

As discussed above with respect to limitation 11[b], charges are accumulated on holding capacitor 60 based on the application of Ivideo, which corresponds to particular image data. Ex. 14, ¶ [0013].

The light emission drive current that flows through the OLED 40 corresponds to the voltage between the gate and source of the light emission control section (i.e., drive transistor), referred to as Vgs. Ex. 14, ¶ [0018] ("Then the voltage between the gate and source, Vgs is stored in the holding capacitor 60 and this storage voltage Vgs keeps" the signal current Ivideo, flowing to the driving TFT 50.").

Vgs is determined by the electric charges previously accumulated on holding capacitor 60 (i.e., the claimed electric charge accumulating section), and thus the light emission drive current is predetermined in accordance with the electric charges. Ex. 14, ¶ [0016] ("At this time, a voltage between the gate and source, Vgs is applied between the gate and Source of the driving TFT 50, which is required for the signal current Ivideo to flow. The voltage is stored in the holding capacitor 60").

iv. Kimura II discloses that the light emission control section "suppl[ies] the "light emission drive current to the light emission element."

As shown in Fig. 33 below, Kimura II discloses that the light emission control section (driving TFT 50) supplies the light emission drive current (signal current Ivideo) to the light emission element (OLED 40). Ex. 14, ¶ [0018] ("After that, the select TFT 51 is turned OFF and a light emitting TFT 52 is turned ON as shown in FIG. 33. Thus, the signal current Ivideo starts flowing to the OLED 40."), [0018] ("Then the voltage between the gate and source, Vgs is stored in the holding capacitor 60 and this storage voltage Vgs keeps the signal current Ivideo, flowing to the driving TFT 50. . . Thus, the signal current Ivideo starts flowing to the OLED 40.").

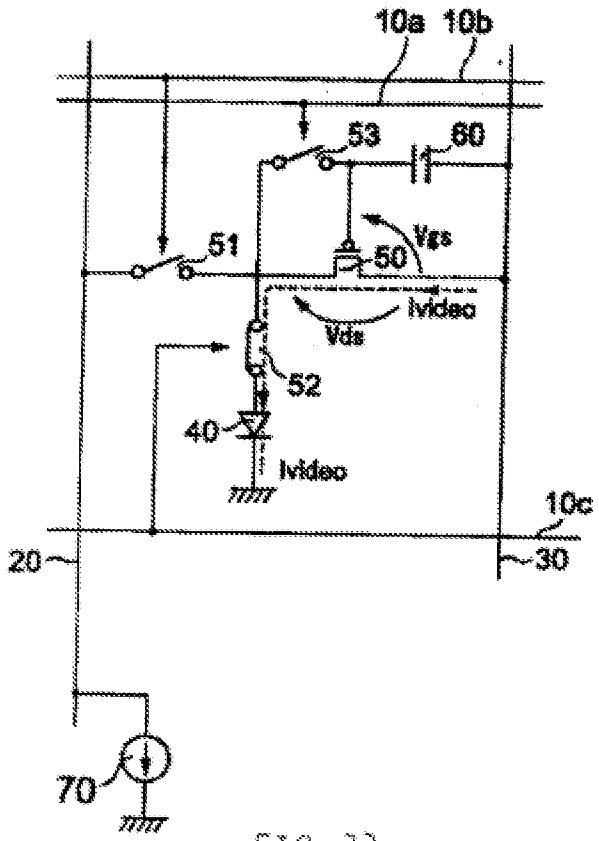


FIG. 33

With regard to claim 11, further teaching ***(d) a writing control section for controlling a supplying state of the electric charges based on the gradation sequence signal to the electric charge accumulating section***,

i. Kimura II discloses a "writing control section" as part of its "light emission drive circuit."

As discussed in Section IX.A.5 of the Request, Kimura II discloses a "writing control section" under either previously asserted construction.

As shown below in Fig. 30, Kimura II discloses a "writing control section" (i.e., select TFT 51) included in its light emission drive circuit (i.e., elements 50-53, 60):

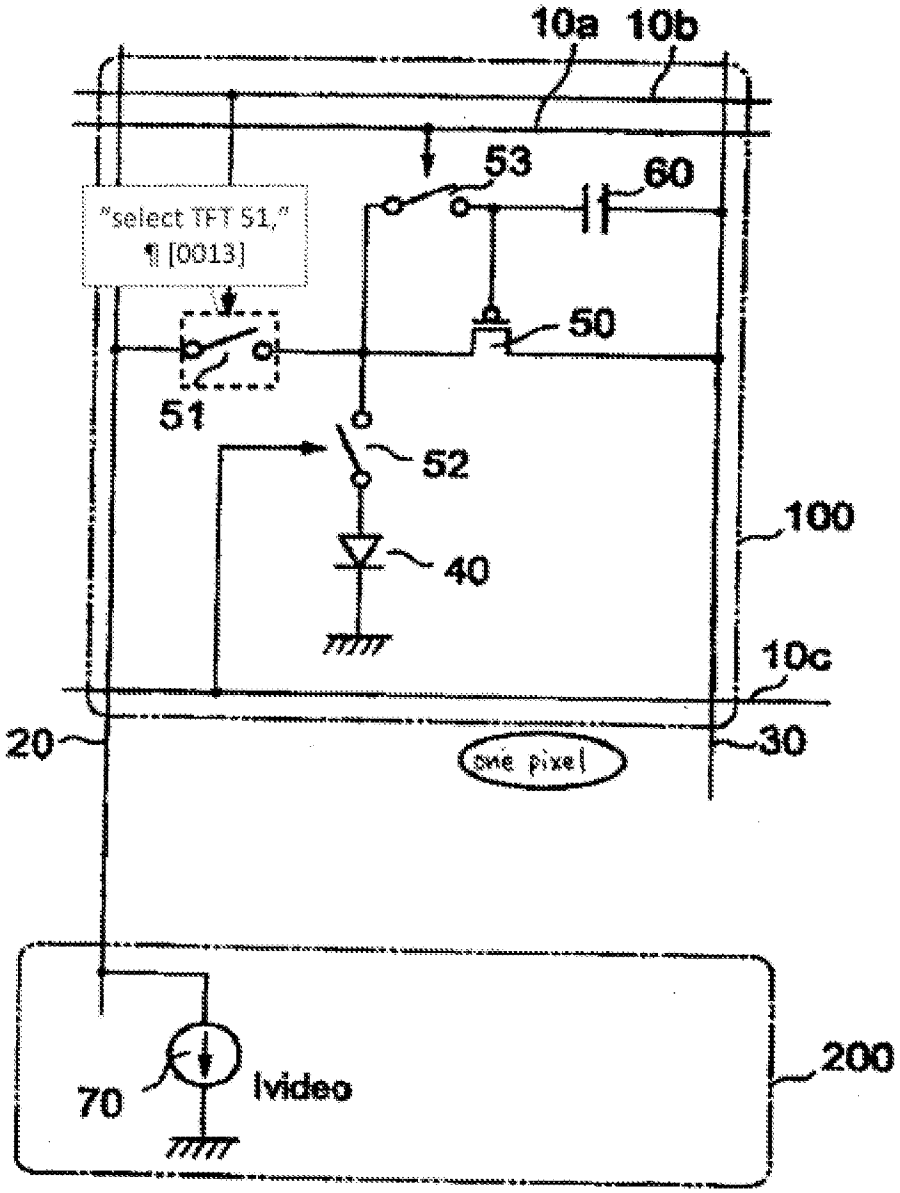


FIG. 30

Ex. 14, Fig. 30 (annotations added).

Select TFT 51 controls the writing of both the gradation sequence signal (Ivideo) and the precharge voltage (Vp) from a data line (signal line 20). Ex. 14, ¶¶ [0015] ("First, as shown in FIG. 31, ... the select TFT 51 [is] turned ON... Then, the signal current Ivideo, ... flows... through . . . the select TFT51 as shown by a dotted line in FIG.31."), [0218], [0222], Fig. 19.

ii. Kimura II discloses that the writing control section "control[s] a supplying state of the electric charges based on the gradation sequence signal to the electric charge accumulating section."

As discussed above in connection with limitation [11b], Kimura II discloses a "gradation sequence signal" in the form of signal current Ivideo. Ex. 14, ¶ [0015]. The select TFT 51 (i.e., the claimed writing control section) controls the supplying state of electric charge based on to the electric charge accumulating section (i.e., holding capacitor 60) based on signal current Ivideo. Ex. 14, ¶¶ [0015] ("First, as shown in FIG. 31, the holding TFT 53 and the select TFT 51 are turned ON . . Then, the signal current Ivideo . . . flows from the power supply line 30 through the driving TFT 50 and the select TFT 51 as shown by a dotted line in FIG. 31."), [0018] ("Then the voltage between the gate and source, Vgs is stored in the holding capacitor 60.").

With regard to claim 11 further teaching ***(e) a voltage control section for controlling a drive voltage for making the light emission control section perform the operation, respectively***;

As shown below in Fig. 30, Kimura II discloses a "voltage control section" (i.e., holding TFT 53) included in its light emission drive circuit (i.e., elements 50-53, 60):

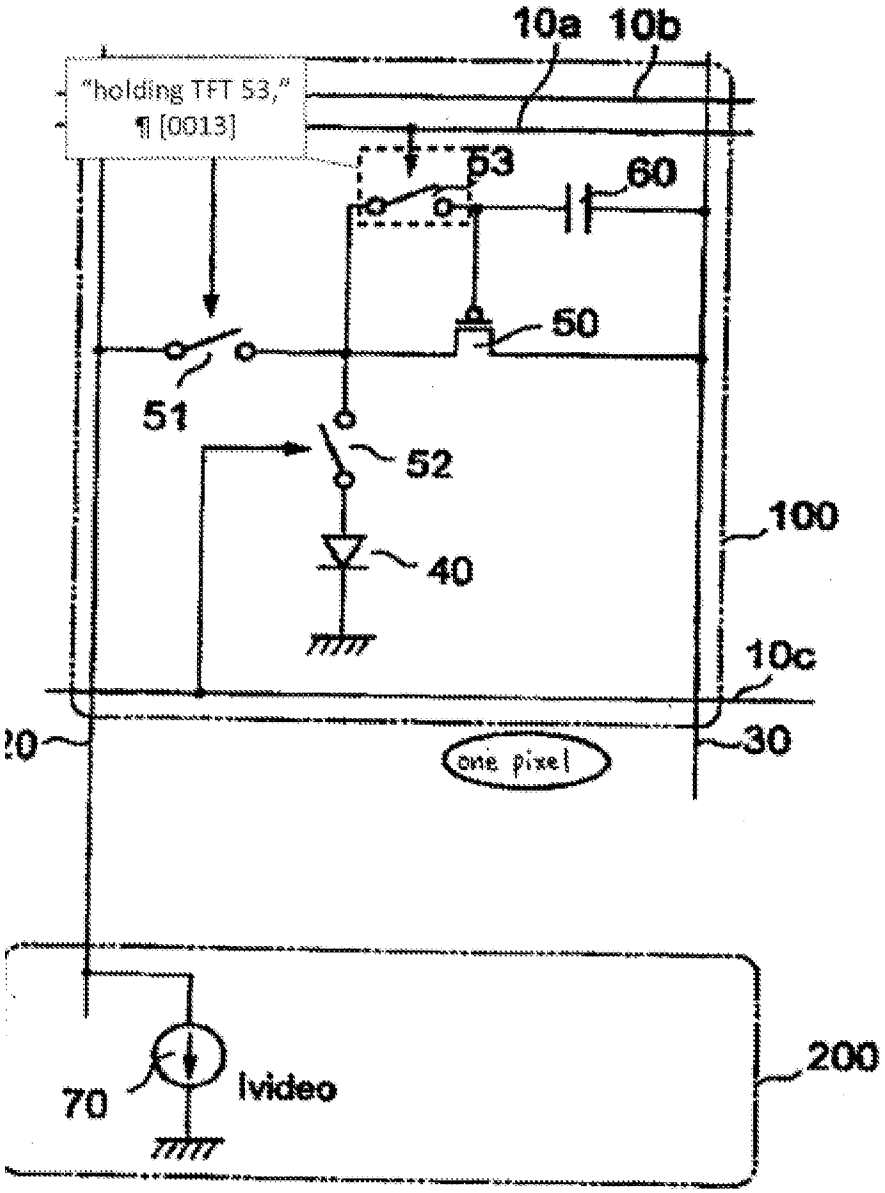


FIG. 30

Ex. 14, Fig. 30 (annotations added); see also id., J [0015].

ii. Kimura II discloses that its voltage control section "control[s] a drive voltage for making the light emission control section perform the operation."

As discussed in Section IX.A.3 of the Request, Patent Owner has stated that "the operation" refers to "generating a light emission drive current having a predetermined current value in accordance with the electric charges accumulated in the electric charge accumulating section and supplying the light emission drive current to the light emission element."

As discussed in Section IX.A.3 of the Request, Requester submits that the broadest reasonable interpretation of "the operation" should include the above functionality. Holding TFT 53 is used to "control[] a drive voltage for making the light emission control section perform the operation," as claimed. As discussed above in connection with limitation [11c], the light emission control section (driving TFT 50) performs the "operation," by supplying a light emission drive current to the light emission element. Ex. 14, ¶¶ [0018] ("After that, the select TFT 51 is turned OFF and a light emitting TFT 52 is turned ON as shown in FIG. 33. Thus, the signal current Ivideo starts flowing to the OLED 40."), [0018] ("Then the voltage between the gate and source. Vac is stored in the holding capacitor 60 and this storage voltage Vgs keeps the signal current Ivideo, flowing to the driving TFT 50... Thus, the signal current Ivideo Starts flowing to the OLED 40.").

Holding TFT 53 controls the value of the voltage being held by the holding capacitor 60 (i.e., the claimed "electric charge accumulating section") on the gate of the driving TFT 50 (i.e., the "light emission control section"), and thereby "controls a drive voltage for making the light emission control section perform the operation." Ex. 14, ¶¶ [0017]-[0018] ("Next, as shown in FIG. 32, the holding TFT 53 is turned OFF. Then the voltage between the gate and source, Vgs is stored in the holding capacitor 60 and this storage voltage Vgs keeps the signal current Ivideo flowing to the driving TFT 50.").

With regard to claim 11, further teaching ***(f) selection lines in which writing control signals for controlling the operation state of the writing control sections of the display pixels are applied***; Kimura II discloses "selection lines" (i.e., control line 10b):

Referring to Fig. 30 below, Kimura II discloses a control line 10b (i.e., a "selection line") that is connected to the gate of select TFT 51 (i.e., the claimed "writing control section"). Ex. 14, ¶ [0015]. .

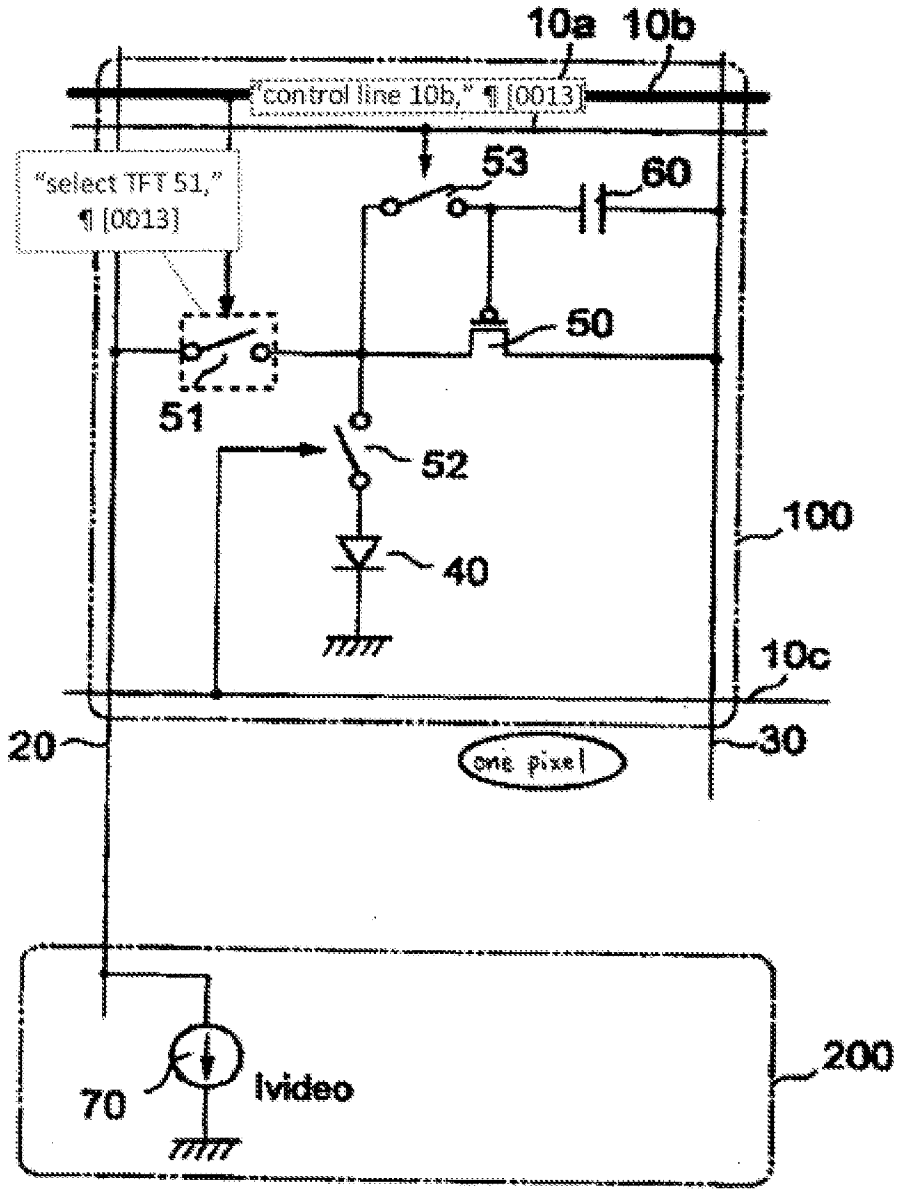


FIG. 30

Ex. 14, Fig. 30 (annotations added). Kimura II discloses that its displays will have a plurality of pixel circuits 100 (as shown above) "disposed in matrix." Ex. 14, ¶ [0012]. Accordingly, a plurality of selection lines would be used, one for each row of pixels.

The control lines 10b (selection lines) "control[] the operational state of the writing control section" (i.e., select TFT 51) using "writing control signals." (i.e., control voltage). Ex. 14, J [0015] ("select TFT 51 [is] turned ON by the control voltage applied to the control line[] 10b.").

With regard to claim 11, further teaching ***(g)*** **hold lines in which voltage control signals for controlling the operation state of the voltage control sections of the display pixels are applied**; Referring to Fig. 30 below, Kimura II discloses a control line 10a (i.e., a "hold line") that is connected to the gate of holding TFT 53 (i.e., the claimed "voltage control section"). Ex. 14, ¶ [0015].

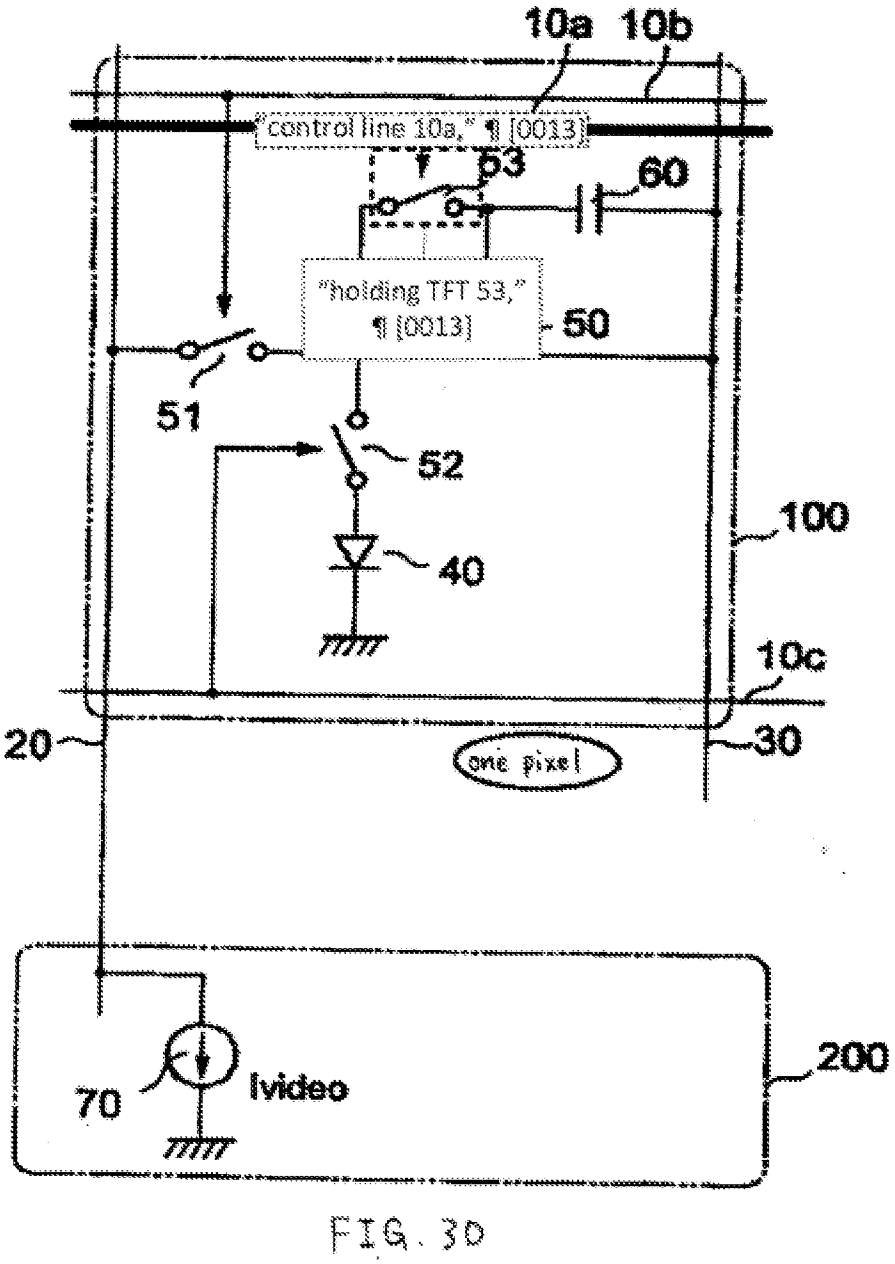


FIG. 30

Ex. 14, Fig. 30 (annotations added). Kimura II discloses that its displays will have a plurality of pixel circuits 100 (as shown above) "disposed in matrix." Id., ¶ [0012].

Accordingly, a plurality of hold lines would be used, one for each row of pixels.

The control lines 10a (hold lines) "control[] the operational state of the voltage control section" (i.e., holding TFT 53) using "voltage control signals." (i.e., control voltage). Ex. 14, ¶ [0015] ("holding TFT 53... [is] turned ON by the control voltage applied to the control line[] 10a.").

With regard to claim 11, further teaching ***(h)* data lines to which the gradation sequence signals are supplied**; As discussed in Section IX.A.6 of the Request, Kimura II discloses "data lines" under either previously asserted construction.

Referring to Fig. 30 below, Kimura II discloses a signal line 20 (i.e., a "data line") connected to the first electrode of the select TFT 51. Ex. 14, ¶ [0015].

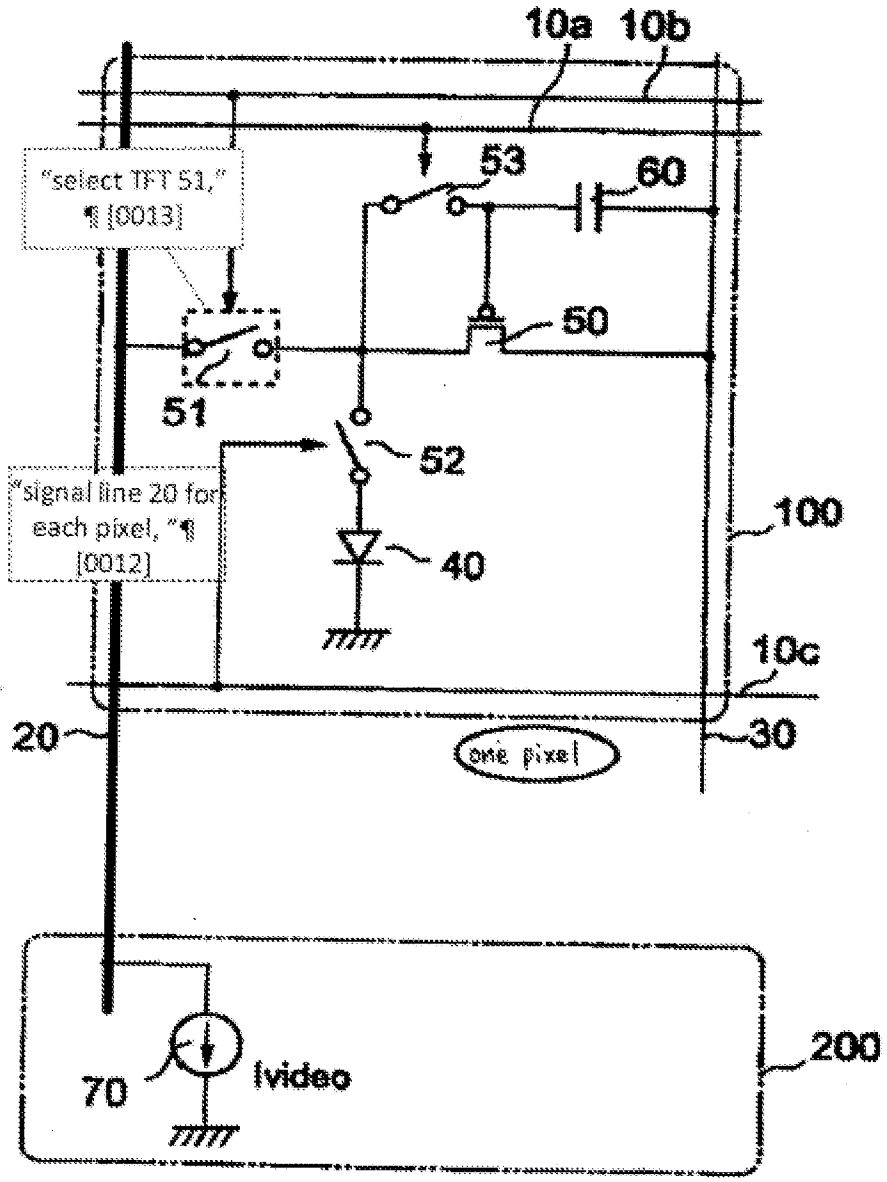


FIG. 30

Ex. 14, Fig. 30 (annotations added).

Signal line 20 is a conductive line. It conveys electrical signals, and it transmits those electrical signals to a plurality of light emission drive circuits. Id., ¶ [0012] ("A signal current having a signal level corresponding to the image data is supplied through a

signal line 20 for each pixel'). Kimura II discloses that its displays will have a plurality of pixel circuits 100 (as shown above) "disposed in matrix." Ex. 14, ¶ [0012]. Accordingly, a plurality of data lines would be used, one for each column of pixels.

Signal lines 20 further supply a "gradation sequence signal" in the form of signal current Ivideo to the writing control sections (i.e., select TFT 51) of the various pixels. Id., ¶¶ [0012]-[0014] ("A signal current having a signal level corresponding to the image data is supplied through a signal line 20 for each pixel"), Fig. 30.

For at least these reasons, Kimura II discloses this limitation.

With regard to claim 11, further teaching ***(i)* a selection driver which applies the writing control signals in the selection lines;** Kimura II teaches a "selection driver" (i.e., gate driver circuit 3502).

As discussed above in connection with limitation [11f], Kimura II discloses applying writing control signals to selection lines. Ex. 14, ¶ [0013] ("a select TFT 51 which switches between ON and OFF corresponding to a control voltage of a control line 10b").

Fig. 35 of Kimura II (shown below) discloses a gate driver circuit 3502:

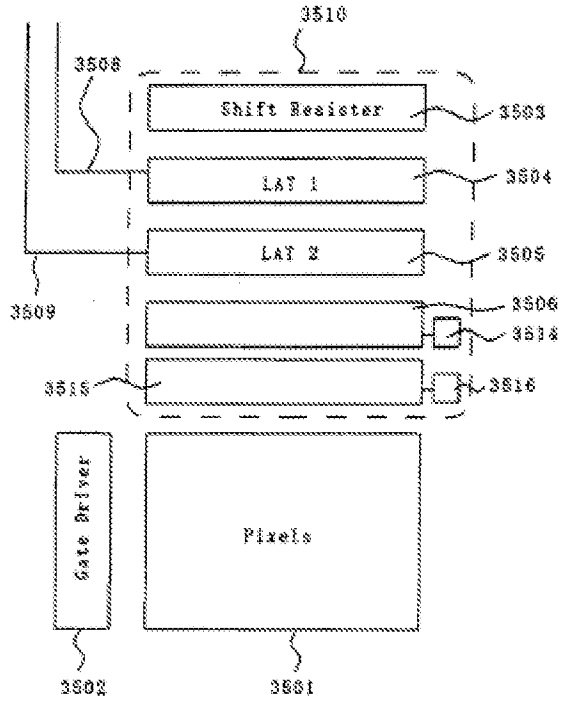


FIG. 35

Ex. 14, Fig. 35. Kimura II discloses that the embodiment described in Figs. 18-20 can be implemented in Fig. 35's pixels 3501. Id., ¶ [0264] ("Next, a display device and a configuration of the signal driver circuit and the operation thereof are described. A circuit of the invention can be applied to a part or a pixel of the signal driver circuit.").

Kimura II discloses the gate driver circuit 3502 outputs control signals sequentially. Ex. 14, ¶ [0265] ("The gate drive circuit 3502 outputs a selection signal to the pixel arrangement 3501 sequentially.") In addition, Kimura II discloses that multiple gate driver circuits can be used. Id., ¶ [0266] ("It should be noted that a plurality of the gate driver circuits 3502 . . . may be provided.").

Kimura II does not expressly disclose that the gate driver circuit 3502 is a "selection driver" because it does not expressly disclose that the claimed "writing control signals" are output by the gate driver circuit 3502 and transmitted to the claimed "selection lines" (i.e., control line 10b) to control the operational state of select TFT 51. Ex. 14, ¶¶ [0013], [0265]. However, a POSITA would have found it obvious to utilize the gate driver circuit 3502 as the claimed "selection driver" for this purpose.

First, a POSITA looking to implement the teachings of Figs. 18-20 would understand that it would require additional circuitry to manipulate the voltage applied to control line 10b in order to change the operational state of the claimed "writing control section" (i.e., select TFT 51) by applying differing voltages to the gate of select TFT 51. Ex. 14, ¶¶ [0013], [0265]; Ex. 19, ¶ [0043].

Second, a POSITA would understand that a driver circuit, such as the gate selection driver 3502 was a well-known and conventional technique used to transmit control signals to transistors in order to modify their operational states. Ex. 19, ¶¶ [0027]-[0030], ¶ [0045]; Ex. 18 at 72 ("Electrically, the OLED's drive requirements are so similar to those of the LCD that it is expected that many LCD production lines could be converted: to OLED production in a reasonably straightforward and economical manner.").

Thus, implementing the claimed "selection driver" to apply the writing control signals in the selection lines, as claimed, would be nothing more than combining prior art

elements (i.e., the gate selection driver 3502 and the control line 10b described in Figs. 18-20 of Kimura II) according to known methods to yield predictable results.

M.P.E.P. § 2143; KSR Int'l Co. v. Teleflex Inc., 550 U.S. 398, 415-421 (2007); Ex. 14, ¶¶ [0013], [0265], [0266]; Ex. 19, ¶¶ [0041]-[0046].

In addition, implementing the gate driver circuit 3502 with Figs. 18-20 would be nothing more than applying a known technique (i.e., a gate selection driver) to a known device (i.e., control line 10b described in Figs. 18-20 of Kimura II) to obtain predictable results (i.e., the operational state of select TFT 51 being controlled by the signals sent by the gate selection driver 3502). M.P.E.P. § 2143; KSR Int'l Co. v. Teleflex Inc., 550 U.S. 398, 415-421 (2007); Ex. 14, ¶¶ [0013], [0265], [0266]; Ex. 19, ¶¶ [0041]-[0046].

A POSITA would also have a reasonable expectation of success implementing a selection driver to apply the writing control signals to the selection lines because it was a well-known technique with predictable results—it would supply the writing control signals at the appropriate timing as explained in connection with the discussion of Figs. 30-32. M.P.E.P. § 2143; KSR Int'l Co. v. Teleflex Inc., 550 U.S. 398, 415-421 (2007); Ex. 14, ¶¶ [0013], [0265], [0266]; Ex. 19, ¶ [0046].

With regard to claim 11, further teaching ***(j)*** **a hold driver which applies the voltage control signals in the hold lines**; Kimura II teaches a "hold driver" (i.e., gate driver

circuit 3502). Gate driver circuit 3502 is the claimed "selection driver" (as discussed above for limitation 11[i]), as well as the claimed "hold driver."

As discussed above in connection with limitation [11g], Kimura II discloses applying voltage control signals to hold lines. Ex. 14, ¶ [0013] ("a holding TFT 53 which switches between ON and OFF corresponding to a control signal of the control line 10a").

Fig. 35 of Kimura II (shown below) discloses a gate driver circuit 3502:

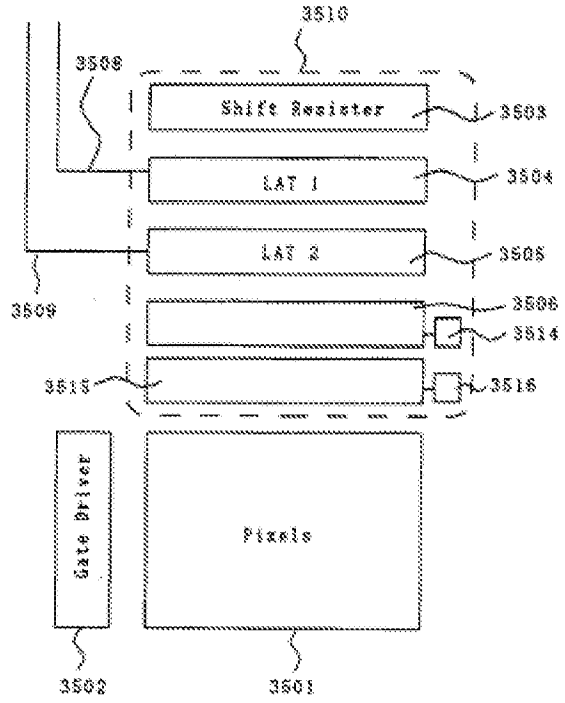


FIG. 35

Ex. 14, Fig. 35. Kimura II discloses that the embodiment described in Figs. 18-20 can be implemented in Fig. 35's pixels 3501. Id., ¶ [0264] ("Next, a display device and a

configuration of the signal driver circuit and the operation thereof are described. A circuit of the invention can be applied to a part or a pixel of the signal driver circuit.").

Kimura II discloses the gate driver circuit 3502 outputs control signals sequentially. Ex. 14, ¶ [0265] ("The gate drive circuit 3502 outputs a selection signal to the pixel arrangement 3501 sequentially."). In addition Kimura II discloses that multiple gate drivers can be used to output different selection signals to the pixel arrangement 3502, even though that is not expressly shown in Fig. 35. Ex. 14, ¶ [0266] ("It should be noted that a plurality of the gate driver circuits 3502... may be provided.").

Kimura II does not expressly disclose that the gate driver circuit 3502 as a "hold driver" because it does not expressly disclose that the claimed "voltage control signals" are output by the gate driver circuit 3502 and transmitted to the claimed "hold lines" (i.e., control line 10a) to control the operational state of holding TFT 53. Ex. 14, ¶¶ [0013], [0265]. However, a POSITA would have found it obvious to utilize a gate driver circuit 3502 as the claimed "hold driver" for this purpose.

First, a POSITA looking to implement the teachings of Figs. 18-20 would understand that it would require additional circuitry to manipulate the voltage applied to control line 10a in order to change the operational state of the claimed "voltage control section" (i.e., holding TFT 53) by applying differing voltages to the gate of holding TFT 53. Ex. 14, ¶¶ [0013], [0265]; Ex. 19, ¶ [0049].

Second, a POSITA would understand that a driver circuit, such as the gate selection driver 3502 was a well-known and conventional technique used to transmit control signals to transistors in order to modify their operational states. Ex. 19, ¶¶ [0027]-[0030], ¶ [0050].; Ex. 18 at 72 ("Electrically. the OLED's drive requirements are so similar to those of the LCD that it is expected that many LCD production lines could be converted to OLED production in a reasonably straightforward and economical manner.").

Thus, implementing the gate driver circuit 3502 as a "hold driver" to apply the voltage control signals to the hold lines, as claimed, would be nothing more than combining prior art elements (i.e., the gate selection driver 3502 and the embodiments described in Figs. 18-20 of Kimura II) according to known methods to yield predictable results. M.P.E.P. § 2143; KSR, 550 U.S. at 415-421; Ex. 14, ¶¶ [0013], [0265], [0266]; Ex. 19, ¶¶ [0047]-[0052].

In addition, implementing the gate selection driver 3502 with the embodiments described in Figs. 18-20 of Kimura II would be nothing more than applying a known technique (i.e., a gate selection driver) to a known device (i.e., control line 10a described in Figs. 18-20 of Kimura II) to yield predictable results (i.e., the operational state of holding TFT 53 being controlled by the signals sent by the gate selection driver 3502). M.P.E.P. § 2143; KSR, 550 U.S. at 415-421; Ex. 14, ¶¶ [0013], [0265], [0266]; Ex. 19, ¶¶ [0047]-[0052].

A POSITA would also have a reasonable expectation of 'success implementing a hold driver to apply voltage control signals to hold lines because it was a well-known technique with predictable results—it would supply the voltage control signals at the appropriate timing as explained in connection with Figs. 30-32. M.P.E.P. § 2143; KSR, 550 U.S. at 415-421; Ex. 14, ¶¶ [0013], [0265], [0266]; Ex. 19, J [0052].

With regard to claim 11, further teaching ***(k)*** **a data driver which supplies the gradation sequence signals to the data lines**; Kimura II discloses this limitation. The image signal input current source 70 corresponds to the claimed "data driver."

As discussed above in connection with limitation [17h], Kimura II discloses supplying "gradation sequence signals" to "data lines" in the form of a signal current Ivideo. Kimura II also discloses a "data driver" which supplies the gradation sequence signals to the data lines. Ex. 14, ¶¶ [0013] ("Further, a source driver circuit 200 has an image signal input current source 70 which outputs a signal current Ivideo having a signal level corresponding to image data."), [0012] ("A signal current having a signal level corresponding to the image data is supplied through a signal line 20 for each pixel"); see also id., ¶¶ [0265]-[0286].

With regard to claim 11, further teaching ***(l)*** **wherein, with respect to each of the display pixels, the data driver applies a precharge voltage exceeding a threshold value of the drive transistor to the data line, and the light emission drive circuit applies the precharge voltage applied to the data line to the electric charge accumulating section via the writing control section,** Kimura II teaches this limitation. For convenience, limitation [11l] is addressed in three parts below.

Note: the '615 Patent specification refers to two separate 'precharge voltages' (see column 19 line 33 through column 20, line 67):

(1) the precharge voltage applied to the data line;

(2) the precharge voltage measured between the opposite ends of the electric charge accumulation section that exceeds a threshold value of the drive transistor.

As discussed in Section VII.B of the Request, the Fig. 30 embodiment is a conventional circuit that Kimura II improves upon by using the techniques described in the embodiment described in Figs. 18-20. Ex. 14, ¶¶ [0204], [0215], which are discussed below.

<u>i. Kimura II discloses that the "data driver applies a precharge voltage . . . to the data line."</u>

Fig. 19 discloses a precharge voltage, where the precharge voltage is applied by the claimed "data driver" to the claimed "data line."

As discussed above, Kimura II discloses a source driver circuit 200 (i.e., the claimed "data driver") that applies a voltage, Vp, (i.e., the claimed "precharge voltage") to the signal lines (i.e., the claimed "data lines"). See limitation [11k], above; see a/so Ex. 14, ¶ [0219] ("the same voltage as the voltage Vp is outputted to an output terminal 86... Thus the signal line 20 and the drain potential of the driving TFT 50 in the pixel circuit 100 reach the precharge voltage Vp').

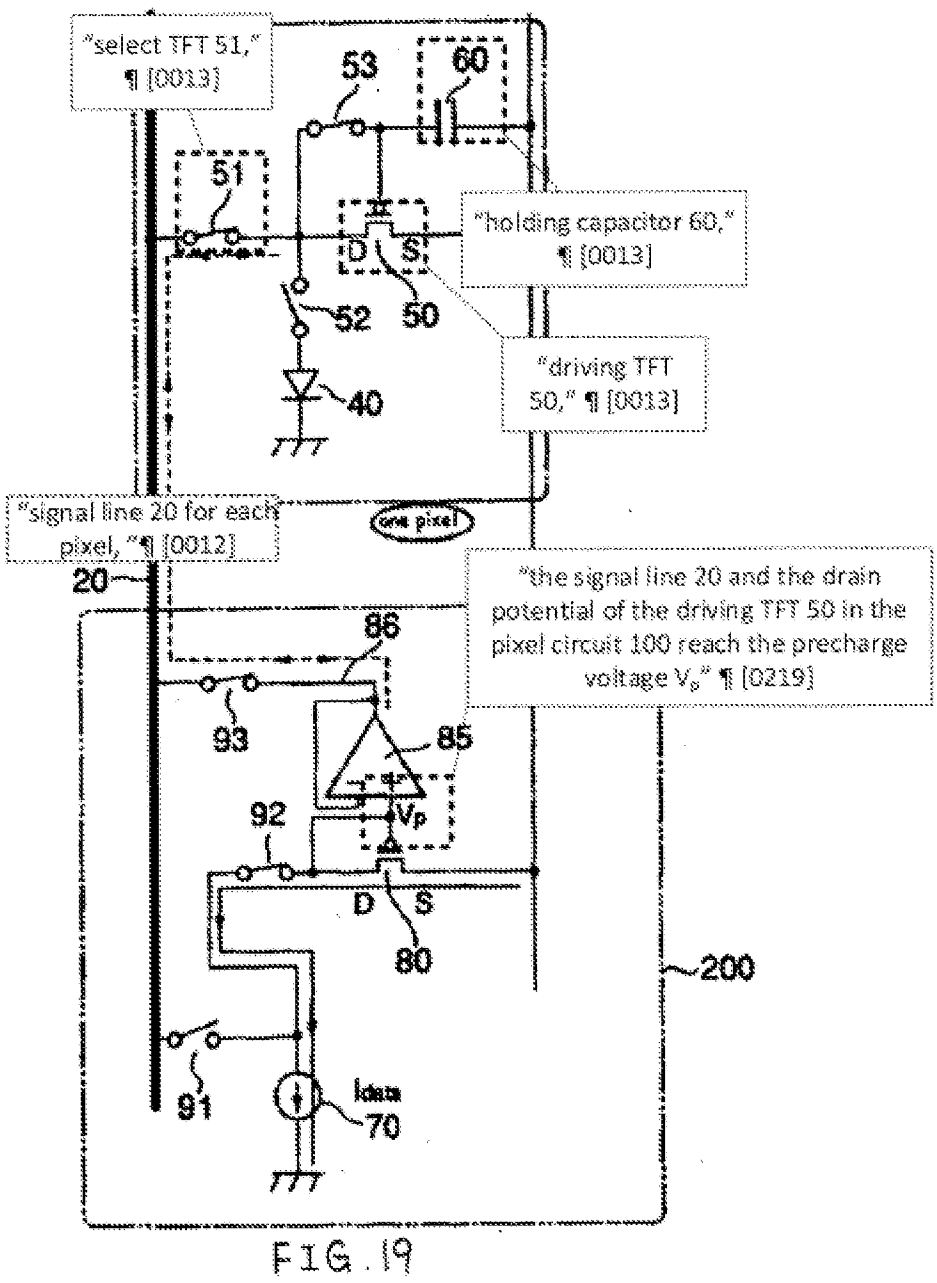


FIG. 19

Ex. 14, Fig. 19 (annotations added).

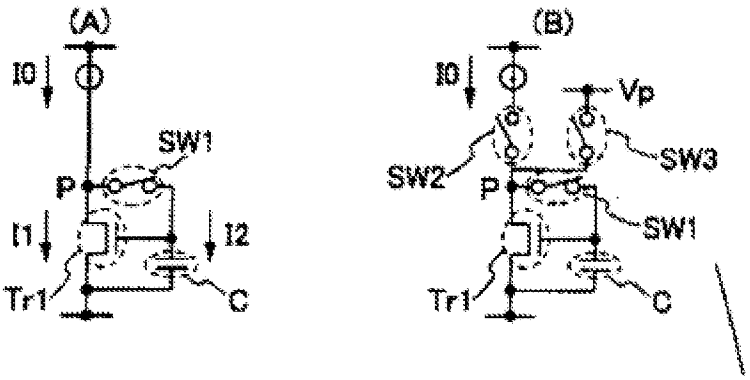
Referring to Fig. 19 above, Kimura II discloses a pre-charge period. Ex. 14, ¶ [0216] ("FIG. 19 shows a signal input operation in a pre-charge period."). During this precharge period, Vp is transmitted by the claimed "data driver" to the light emission drive circuit

via the claimed "data line." Ex. 14, ¶ [0219] ("the same voltage as the voltage Vp is outputted to an output terminal 86... Thus the signal line 20 and the drain potential of the driving TFT 50 in the pixel circuit 100 reach the precharge voltage Vp").

ii. Kimura II discloses that the precharge voltage "exceeds the threshold value of the drive transistor."

Kimura II further discloses that the precharge voltage, Vp, applied to the data line (i.e., signal line 20) exceeds the threshold value of the drive transistor, driving TFT 50, for at least the following reasons.

First, Kimura II discloses that it is desirable to make the potential of the driving TFT 50 in Fig. 19 a steady state via a precharge voltage. Ex. 14, ¶ [0224] ("That is to say, it is desirable to make a potential of a driven element in a pixel circuit in a steady state or a state close to it by a precharge circuit and supply it."). Second, Figs. 9 of Kimura II demonstrates the benefits of applying a precharge voltage to a circuit such as the one shown in Fig. 19. Id., ¶¶ [0099]-[0101]. Referring to Figs. 9(A) and 9(B) below, Kimura discloses a node P that is located at a terminal of the transistor Tr1 and is - electrically connected via a switch or transistor element to the gate of the same transistor Tr1 in identical fashion to the driving TFT 50 of Fig. 19. Id., ¶¶ [0013], [0099], Figs. 9(A), 9(B), 19; Ex. 19, ¶¶ [0054]-[0056].



Ex. 14, Figs. 9(A), 9(B).

Thus, a POSITA would understand that transistor Tr functions in the same manner as driving TFT 50 in Fig. 19, or at the very least that operating driving TFT 50 in the same manner as transistor Tr: would be nothing more than the application of a known technique to a known device ready for improvement to yield predictable results. Id., ¶¶ [0012], [0099]; Ex. 19, ¶¶ [0054]-[0056]; M.P.E.P. § 2143; KSR, 550 U.S. at 415-421.

Third, Kimura II discloses that the precharge voltage is applied to node P to reach the steady state voltage faster than when a precharge is not applied, and that the precharge voltage exceeds the threshold voltage of the drive transistor. Ex. 14, ¶ 0099]-[0104].

In particular, Fig. 9(D), reproduced below, shows a voltage change at node P according to time. Id., ¶ [0099]. As shown, the steady state voltage exceeds the threshold voltage, Vth.

Fig. 9(E), also reproduced below, illustrates the use of a precharge voltage, and demonstrates that the precharge voltage is close, if not equal, to the steady state voltage. In particular. Kimura II discloses that the precharge voltage is desirably the same value as the steady state voltage in order to reduce the amount of time needed to reach steady state. Ex. 14, ¶ [0102] ("the precharge voltage is desirably the same potential as the potential of node P in a steady state"); id., ¶ [0103] ("When the precharge is performed then, the transistor Tr1 becomes a steady state in a short time.").

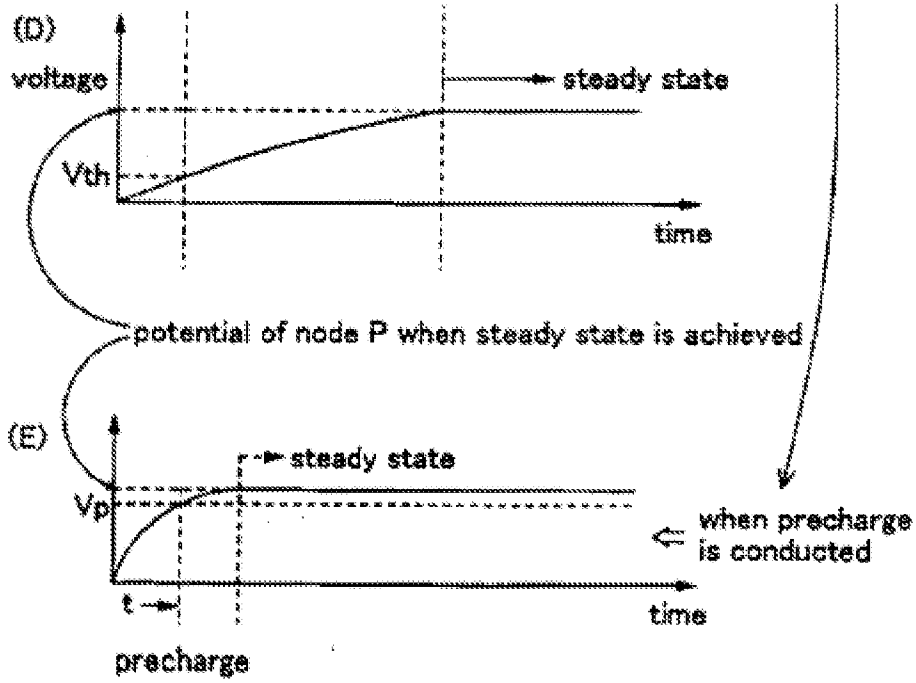


FIG. 9

Ex. 14, Fig. 9(D), 9(E); see also id., ¶¶ [0099]-[0100].

Because Kimura II teaches that transistor Tr; functions in the same manner as driving TFT 50, and because Kimura II discloses that the voltage at node P when steady state

is achieved exceeds the threshold value of transistor Tri, Kimura II teaches that the precharge voltage applied to the signal line 20 exceeds the threshold value of the driving TFT 50. Ex. 19, ¶¶ [0054]-[0056]; M.P.E.P. § 2143; KSR, 550 U.S. at 415-421.

iii. Kimura II discloses that the light emission drive circuit "applies the precharge voltage applied to the data line to the electric charge accumulating section via the writing control section."

Kimura II discloses that the precharge voltage is "applied to the electric charge accumulating section of the light emission drive circuit via the writing control section," as claimed. Still referring to Fig. 19, reproduced again below, Kimura discloses that Vp is transmitted to Kimura's pixel circuit 100 (i.e., the claimed light emission drive circuit), via select TFT 51 (i.e., the claimed writing control section), after which it is applied to the holding capacitor 60 (i.e., the claimed electric charge accumulating section). Ex. 14, ¶ [0219], Fig. 19.

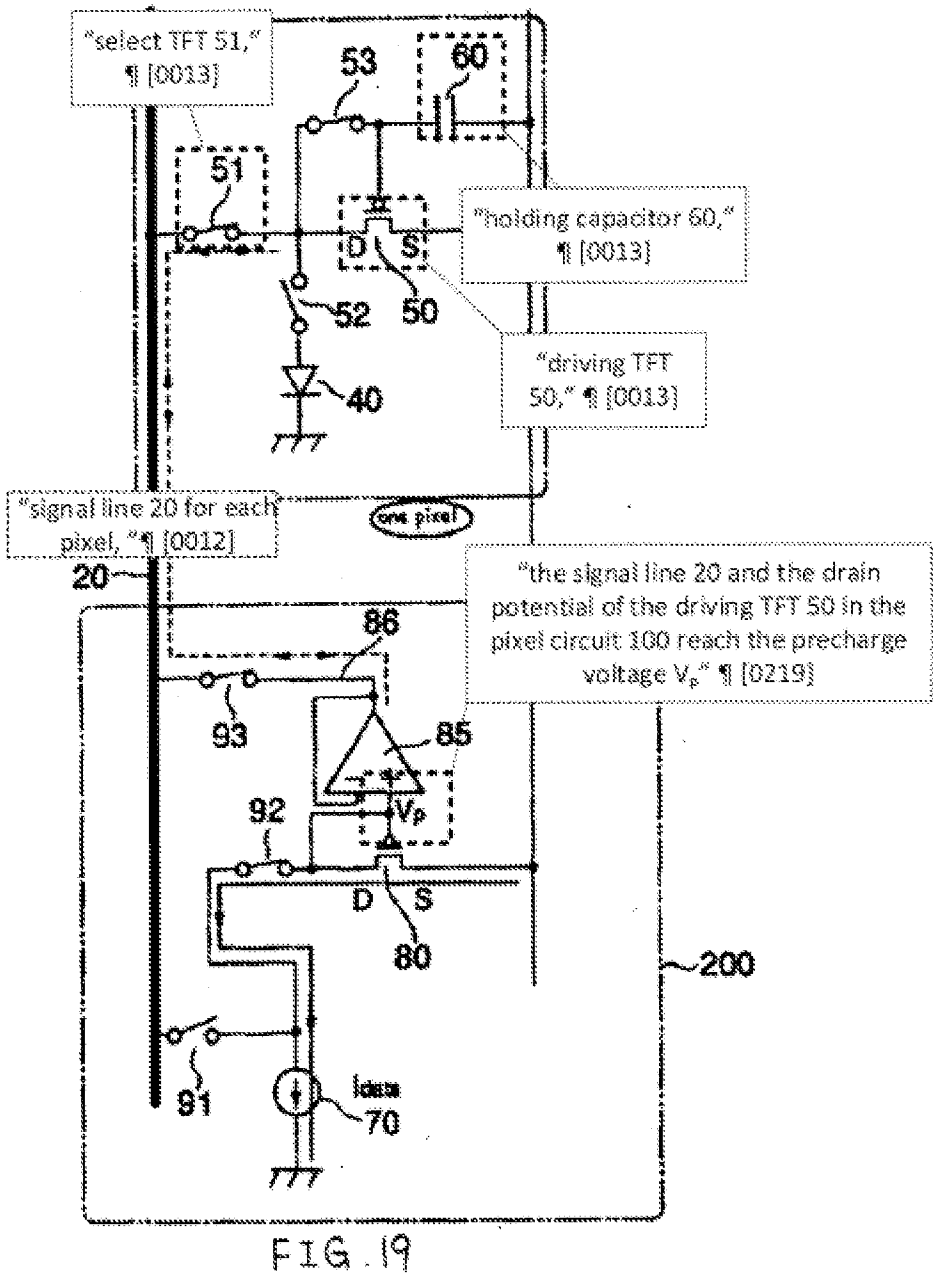


FIG. 19

Ex. 14, Fig. 19 (annotations added).

With regard to claim 13, further teaching ***wherein the precharge voltage and the gradation sequence signal applied from the data driver to the data line are applied in the electric charge accumulating section via the writing control section at different timings, respectively,*** As discussed above in connection with claim 11, Kimura II discloses each and every limitation of claim 11. See Section IX.C.2.a of the Request.

Kimura II discloses the additional limitation recited in claim 13.

As described above in connections with limitations [11b], [11d], [11h], and [11k], Kimura II discloses that a "data driver" applies "gradation sequence signals' (i.e., Idata/Ivideo in Kimura I) to the data line, and that those gradation sequence signals are applied to the electric charge accumulation section via the writing control section.

Also as described above in connection with limitation [11l], Kimura II discloses that a data driver applies a recharge voltage (i.e.. Vp in Kimura II) to the data line, and that the precharge voltage is applied to the electric charge accumulation section via the writing control section.

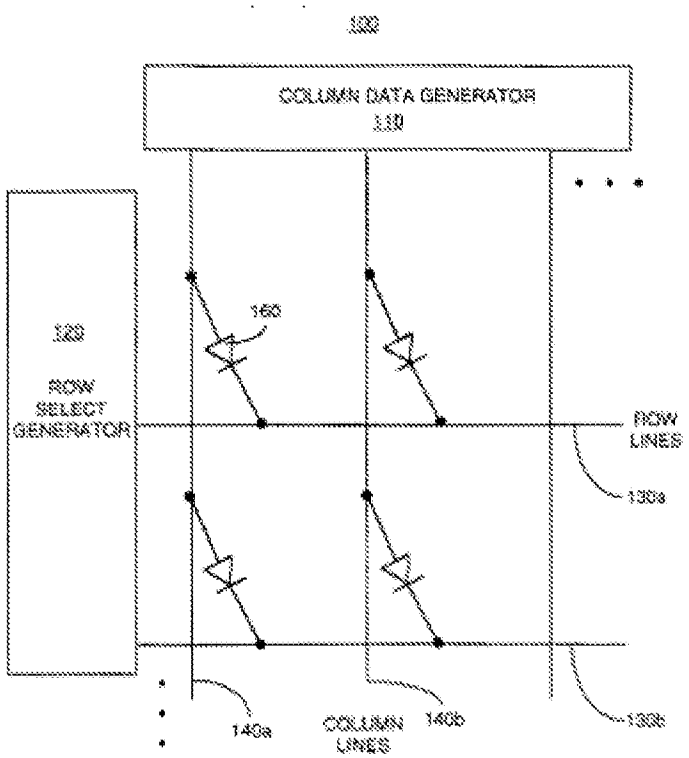
Kimura II discloses that the precharge voltage and gradation sequence signal are applied at different respective timings. That is, Kimura II discloses that the precharge voltage Vp is applied first. Ex. 14, ¶ [0219] ("By using the amplifier 85, the same voltage as the voltage Vp is outputted to an output terminal 86"). After the precharge voltage is

disconnected, Kimura II discloses that the gradation sequence signal is applied. Ex. 14, ¶¶ [0220] ("Then, the switches 92 and 93 are turned OFF and the Switch 91 is turned ON as shown in FIG. 20."), [0221] ("Thus, the output voltage of the amplifier 85 is disconnected and a correct signal based on the signal current Idata from the image signal input source 70 is inputted to the pixel circuit 100.").

C. Dawson

Claims 11 and 13 are rejected under pre-AIA 35 U.S.C. 102 (b) as anticipated by or, in the alternative, under pre-AIA 35 U.S.C. 103(a) as obvious over Dawson (Ex. 15), PCT Publication No.: WO 98/48403 (hereinafter Dawson), as presented on pages 30-35 and 115-147 of the Request and reproduced in part below.

With regard to claim 11, teaching ***(pre) A display unit***; Dawson discloses a "display unit":



(PRIOR ART)

FIG. 1

Ex. 15, Fig. 1. Id., 1:19-20 ("matrix displays are well known in the art, where pixels are illuminated using matrix addressing as illustrated in FIG. 1.").

With regard to claim 11 teaching ***(a) the display unit comprising: a plurality of display pixels each of which includes a light emission element and a light emission drive circuit***, Dawson discloses "a plurality of display pixels." See Ex. 15. 1:20—22 ("A typical display 100 comprises a plurality of picture or display elements (pixels) 160 that are arranged in rows and columns."), Fig. 1.

Dawson also discloses that each display pixel includes "a light emission element and a light emission drive circuit."

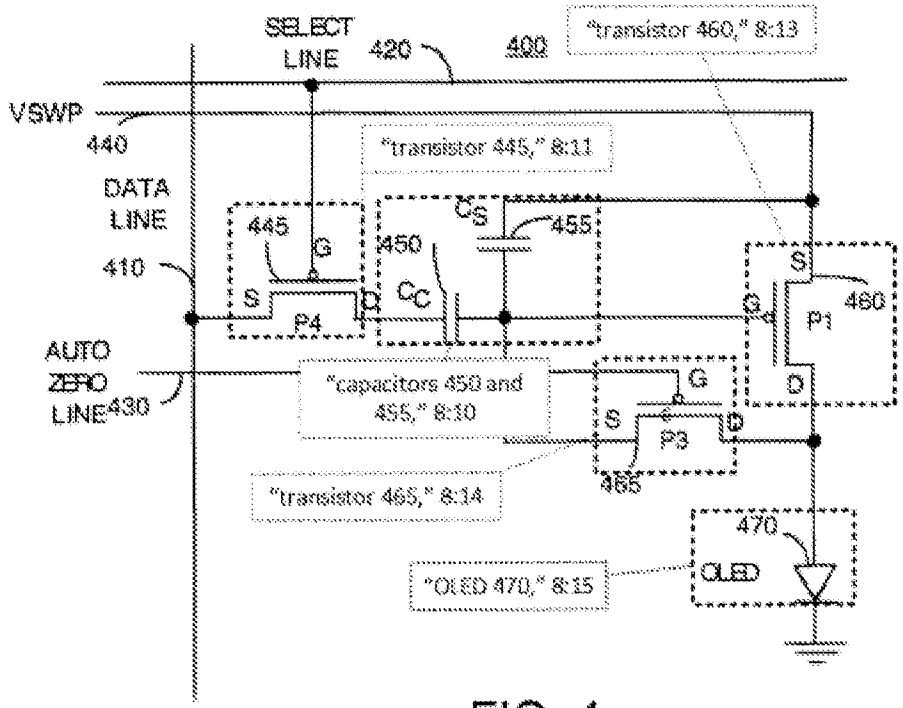


FIG. 4

Ex. 15, Fig. 4 (annotations added), 3:5-6 ("FIG. 4. depicts a schematic diagram of another alternate embodiment of the present active matrix LED pixel structure.").

Referring to Fig. 4 above, Dawson also discloses a light emission element, i.e., an organic light emitting diode, OLED 470. Ex. 15, 8:10.

Fig. 4 also discloses a light emission drive circuit that includes three transistors (445, 460, 465) and two capacitors (450 and 455), which are all connected via wiring shown in the diagram above. Ex. 15, 8:9-10. Dawson's light emission drive circuit is also connected to a select line 420, a data line 410, an auto zero line 430 and a VSWP line 440. Id., 8:9-18; Fig. 4.

With regard to claim 11, ***further teaches (b) the light emission drive circuit having an electric charge accumulating section for accumulating electric charges based on a gradation sequence signal to designate a luminance gradation sequence in accordance with display data***,

Dawson discloses this limitation. For convenience, limitation [11b] is addressed in three parts below.

<u>i. Dawson discloses an "electric charge accumulating section" as part of its "light emission driver circuit."</u>

As discussed in Section IX.A.7 of the Request, Requester submits that the broadest reasonable interpretation of the term "electric charge accumulating section" should include a capacitor.

As shown in Fig. 4 below, Dawson discloses an "electric charge accumulating section" (i.e., capacitors 450 and 455) included in its light emission drive circuit (i.e., elements 445, 450, 455, 460, and 465):

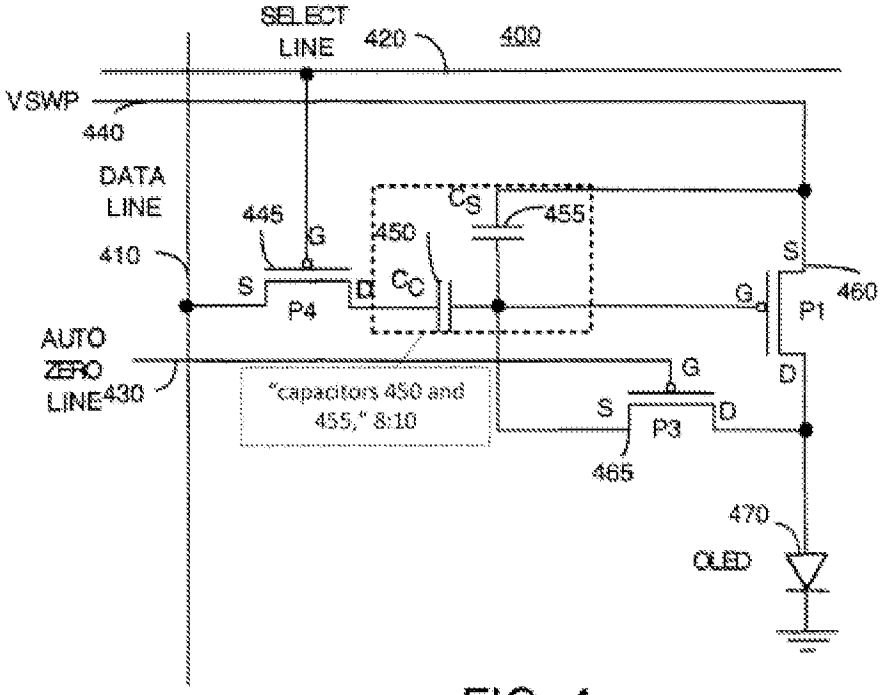


FIG. 4

Ex. 15, Fig. 4 (annotations added).

ii. Dawson discloses a "gradation sequence signal."

As discussed in Section IX.A.1 of the Request, Patent Owner previously agreed that the term "gradation" should be construed as a "level."

Dawson discloses that in its Fig. 4 embodiment, the data line transmits a sequence signal level, i.e., "data voltage." Ex. 15, 9:10-12 ("Next, the data line is then switched from a reference voltage to a lower voltage (data voltage) where the change in the data is referenced to the data.").

iii. Dawson discloses that the electric charge accumulating section "accumulat[es] electric charges based on a gradation sequence signal to designate a luminance gradation sequence in accordance with display data,"

As discussed above, Dawson discloses an electric charge accumulating section, capacitors 450 and 455, and a gradation sequence signal, data voltage. Dawson's data voltage is used to designate "a luminance gradation sequence in accordance with display data," as claimed. Dawson discloses that the data voltage accords with display data. Ex. 15, 9:10-12 ("the change in the data is referenced to the data."). Further, Dawson discloses that the data voltage is used to control the level of light emitted from the OLED, id., 2:23—25 ("Next, a data voltage . . . is now applied to illuminate the pixel.").

Dawson discloses that electric charges "accumulai[e] at the electric charge accumulating section" on the basis of Dawson's data voltage, as claimed. Ex. 15, 9:12-

14 ("In turn, the data voltage (data input) is load coupled through capacitors 450 and 455 to the gate of transistor PI 460.").

The electric charges that accumulate on capacitors 450 and 455 based on the data voltage designate a "luminance gradation [i.e., level] sequence in accordance with display data" by controlling the value of the current (i.e., the luminance level) that flows to the OLED for light emission. Ex. 15, 9:12—16 ("In turn, the data voltage (data input) is load coupled through capacitors 450 and 455 to the gate of transistor PI 460. The voltage Vsg of the transistor 460 provides the transistor PI (460) with a fixed overdrive voltage to drive the current for the OLED 470.").

With regard to claim 11, further teaching ***(c) a light emission drive circuit having a light emission control section for generating a light emission drive current having a predetermined current value in accordance with the electric charges accumulated in the electric charge accumulating section and supplying the light emission drive current to the light emission element,*** Dawson discloses this limitation. For convenience, limitation [11c] is addressed in four parts below.

<u>i. Dawson discloses a "light emission control section" as part of its "light emission drive circuit."</u>

As discussed in Section IX.A.2 of the Request, Patent Owner previously agreed that the term "light emission control section" should be construed as a "drive transistor." Dawson

discloses transistor 460, which serves as a drive transistor. Ex. 15, 8:31 ("transistor PI (460) (drive transistor)') (emphasis added).

As shown in Fig. 5 below, transistor 460 is part of the light emission drive circuit, (i.e., elements 445, 450, 455, 460, and 465)

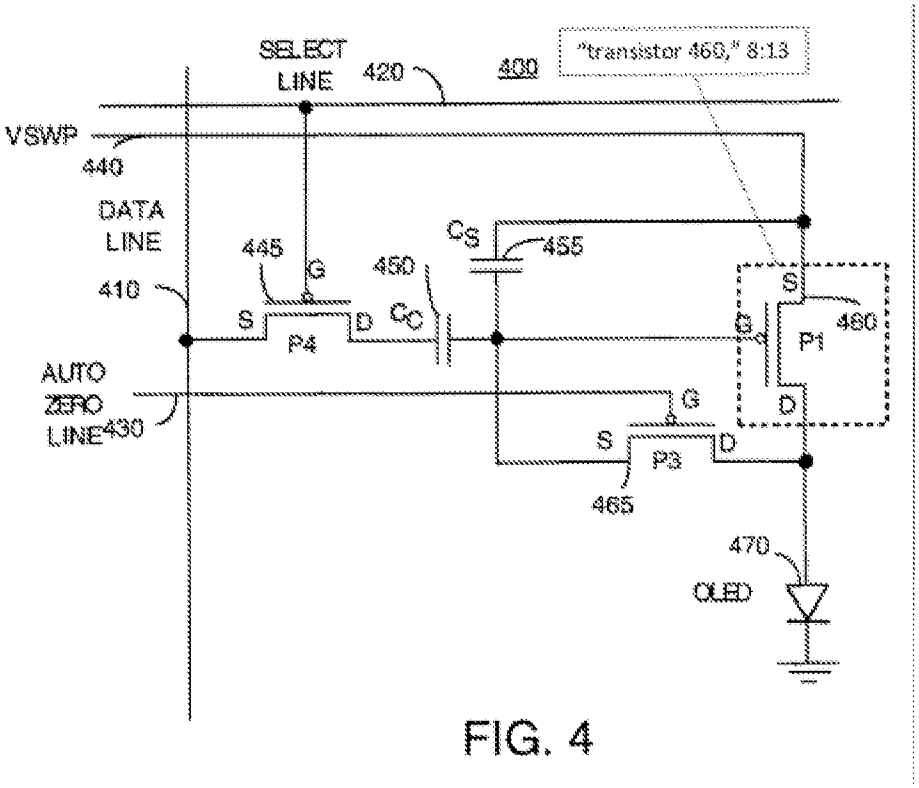


FIG. 4

Ex. 15, Fig. 4 (annotations added).

ii. Dawson discloses that the light emission control section "generat[es] a light emission drive current"

Dawson discloses that the drive transistor 460 (i.e., light emission control section) generates a light emission drive current. Ex. 15, 9:14-16 ("The voltage Vsg of the transistor 460 provides the transistor PI (460) with a fixed overdrive voltage to drive the current for the OLED 470.").

iii. Dawson discloses that the light emission drive current has a "predetermined current value in accordance with the electric charges accumulated in the electric charge accumulating section."

Dawson discloses that the light emission drive current has a predetermined current value in accordance with the electric charges stored on capacitors 450 and 455.

Dawson discloses that the electric charge stored on capacitors 450 and 455 is used to load couple the data voltage to the gate of transistor P1 460 (i.e., the drive transistor), resulting in a voltage, Vsg, on the gate of transistor P1 460. Ex. 15, 9:13—16 ("In turn, the data voltage (data input) is load coupled through capacitors 450 and 455 to the gate of transistor PI 460. The voltage Vsg of the transistor 460 . . ."). The light emission drive current that flows through the OLED 460 corresponds to the voltage between the gate and source of the light emission control section (i.e., transistor 460), represented by Vsg. Id., 9:14-16 ("The voltage Vsg of the transistor 460 provides the transistor PI (460) with a fixed overdrive voltage to drive the current for the OLED 470.") Vsg is determined by the electric charges previously accumulated on capacitors 450 and 455 and thus the light emission drive current is predetermined in accordance with the

electric charges. Id., 9:14—16 ("The voltage Vsg of the transistor 460 provides the transistor PI (460) with a fixed overdrive voltage to drive the current for the OLED 470."); see also id., 9:29-34 ("the data voltage is kept in storage on Vsg of transistor 460 as before. This source-to-gate voltage Vsg (PI) is maintained in the same manner throughout the entire Illumination phase, which means the current level through the OLED will be constant.").

iv. Dawson discloses that the light emission control section "suppl[ies] the light emission drive current to the light emission element."

Dawson discloses that transistor 460 (i.e., the light emission control section) supplies the light emission drive current to the light emission element. Ex. 15, 9:14—16 ("The voltage Vsg of the transistor 460 provides the transistor PI (460) with a fixed overdrive voltage to drive the current for the OLED 470.").

With regard to claim 11, further teaching ***(d) a writing control section for controlling a supplying state of the electric charges based on the gradation sequence signal to the electric charge accumulating section***,

Dawson discloses this limitation. For convenience, limitation [11d] is addressed in two parts below.

i. Dawson discloses a "writing control section" as part of its "light emission drive circuit."

As discussed in Section IX.A.5 of the Request, Dawson discloses a "writing control section" under either previously asserted construction.

As shown below in Fig. 4, Dawson discloses a "writing control section" (i.e., transistor 445) included in its light emission drive circuit (i.e., elements 445, 450, 455, 460, and 465):

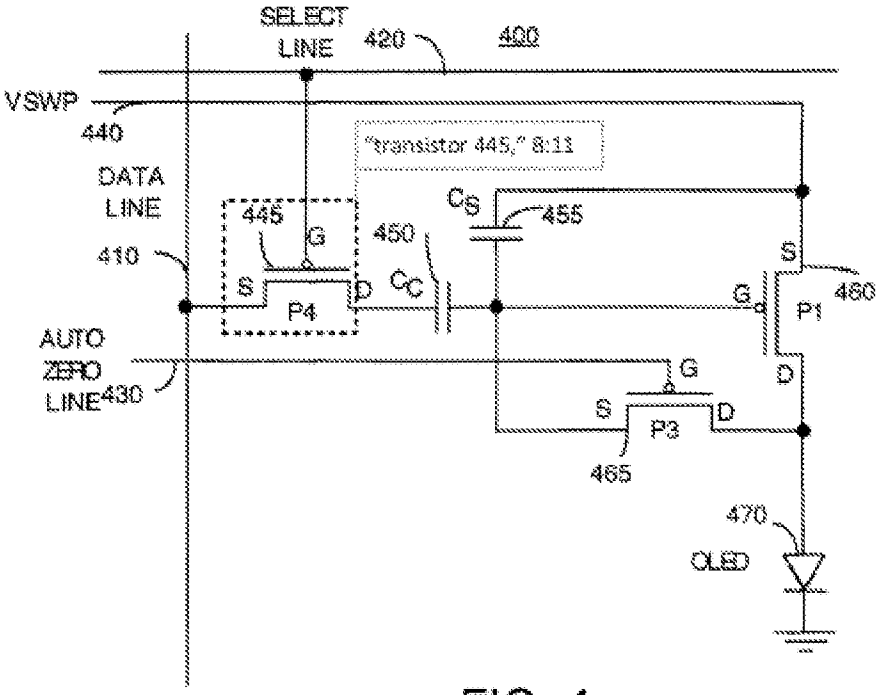


FIG. 4

Ex. 15, Fig. 4 (annotations added).

Transistor 445 controls the writing of both the gradation sequence signal (data voltage) and the precharge voltage (reference voltage) from a data line (data line 410). Ex. 15, 8:32-33 ("The select line 420 is then set to 'Low' and a 'reference voltage' is applied on

the data line 410."), 9:10—12 ("Next, the data line is then switched from a reference voltage to a lower voltage (data voltage) where the change in the data is referenced to the data.").

ii. Dawson discloses that the writing control section "control[s] a supplying state of the electric charges based on the gradation sequence signal to the electric charge accumulating section."

As discussed above in connection with imitation [11b], Dawson discloses a "gradation sequence signal" (data voltage). Ex. 15, 9:10-12 ("Next, the data line is then switched from a reference voltage to a lower voltage (data voltage) where the change in the data is referenced to the data.").

Dawson discloses that its transistor P4 445 (i.e., the claimed writing control section) controls the supplying state of electric charge based on the data voltage to the electric charge accumulating section (i.e., capacitors 450 and 455) by toggling on and off, and thereby supplies a state of electric charge to the charge accumulating section. Ex. 15, 9:9-24 ("At the end of the Auto Zero phase, the select line was set 'Low' and the data line was at a 'reference voltage'. Next, the data line is then switched from a reference voltage to a lower voltage (data voltage) . . . In turn, the data voltage (data input) is load coupled through capacitors 450 and 455 .. The select line 420 is then set "High". This completes the load data phase.").

With regard to claim 11 further teaching ***(e) a voltage control section for controlling a drive voltage for making the light emission control section perform the operation, respectively***;

Dawson discloses this limitation. For convenience, limitation [11e] is addressed in two parts below.

i. Dawson discloses a "voltage control section" as part of its "light emission drive circuit."

Dawson discloses a "voltage control section" (i.e., transistor 465) included in its light emission drive circuit (i.e., elements 445, 450, 455, 460, and 465):

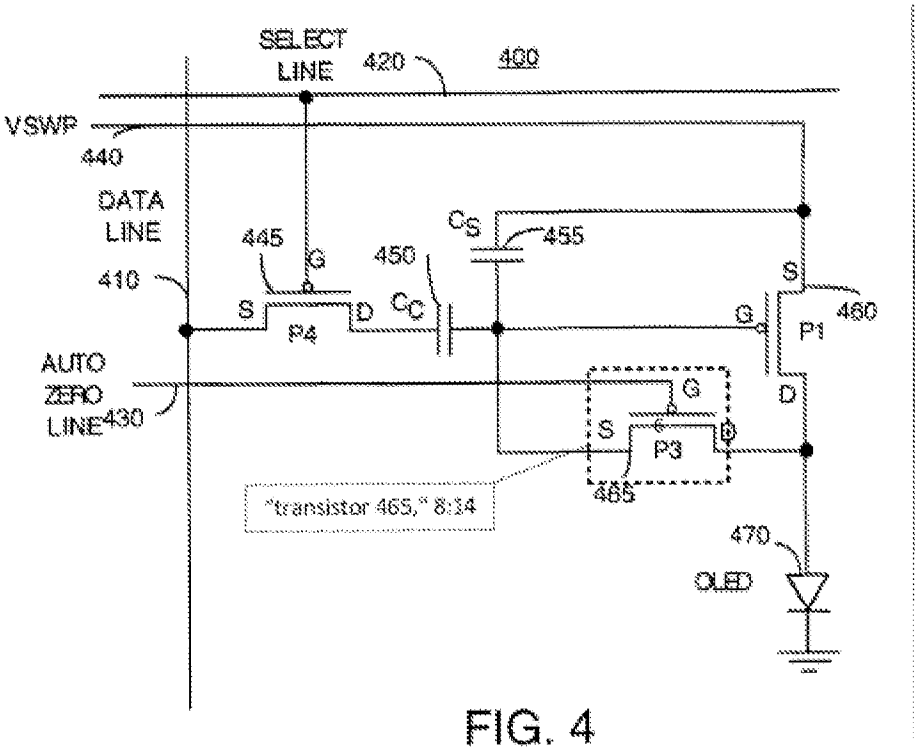


FIG. 4

Ex. 15, Fig. 4 (annotations added); see also id., 8:9-10.

ii. Dawson discloses that its voltage control section "control[s] a drive voltage for making the light emission control section perform the operation."

As discussed in Section IX.A.3 of the Request, Patent Owner has stated that the operation" refers to "generating a light emission drive current having a predetermined current value in accordance with the electric charges accumulated in the electric charge accumulating section and supplying the light emission drive current to the light emission element.

As discussed in Section IX.A.3 of the Request, Requester submits that the broadest reasonable interpretation of "the operation" should include the above functionality. Transistor 465 is used to "control[] a drive voltage for making the light emission control section perform the operation," as claimed.

As discussed above in connection with limitation [11c], Dawson's light emission control section (transistor P1 460) performs the "operation", by supplying a light emission drive current to the light emission element. Ex. 15, 2:23-25 ("Next, a data voltage .. . is now applied to illuminate the pixel.").

Dawson's transistor P3 465 is used to control the voltage being applied to the gate of Dawson's light emission control section (i.e., drive transistor, P1 460), and thereby

controls a drive voltage for making the light emission control section perform the operation:

Finally, Auto Zero line 430 is then set to "High", which isolates the gate of transistor PI 460. The effect of this Auto Zero phase is to store on the capacitor C, 450 a voltage (an auto-zero voltage) that represents the difference between the reference voltage on the data line and the transistor threshold voltage of P1 460.

Ex. 15, 9:2-6, 9:24—26 ("At the completion of the data loading phase, the gate of transistor PI 460 is now isolated except for its capacitive connections, where the overdrive voltage for driving the OLED is stored on capacitor Cs 455."), 9:29-31 ("both transistors P3 (465) and P4 (445) are turned 'Off', and the data voltage is kept in storage on Vsg of transistor 460 as before.").

With regard to claim 11, further teaching ***(f) selection lines in which writing control signals for controlling the operation state of the writing control sections of the display pixels are applied***; Dawson discloses a selection line (i.e., select line 420):

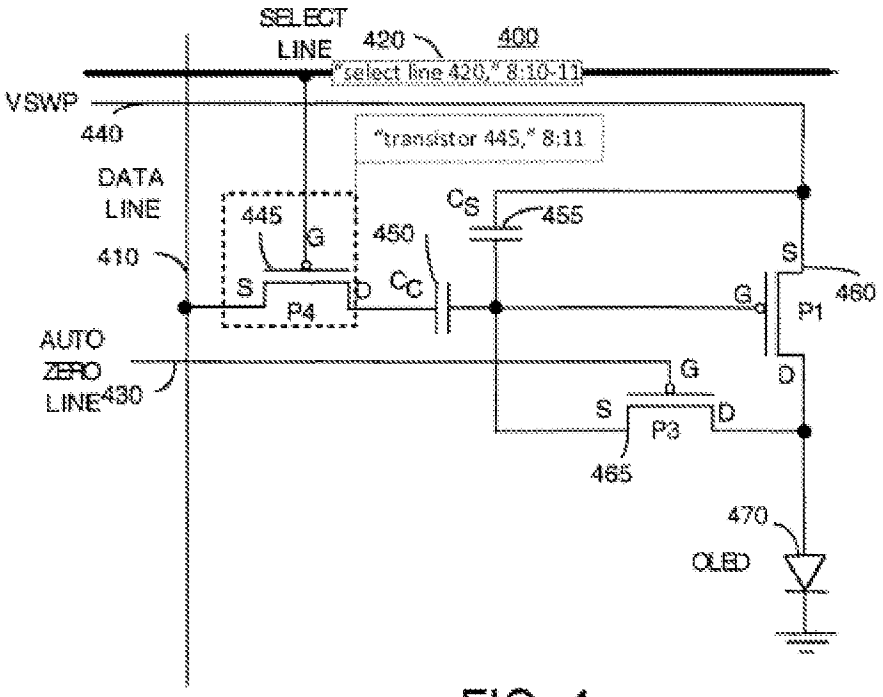


FIG. 4

Ex. 15, Fig. 4 (annotations added).

Referring to Fig. 4 above, Dawson discloses a "select line 420" that is connected to the gate of transistor P4 445. Id., 8:10-11. Dawson's select line is the claimed selection line. Dawson discloses that its displays will have a plurality of pixels arranged in an array. Id., 3:33-35 ("Although the present invention is illustrated below as a single pixel or pixel structure, it should be understood that the pixel can be employed with other pixels, e.g., in an array, to form a display."). Accordingly, Dawson discloses a plurality of selection lines, one for each row of pixels. Id., Fig. 1, 1:19-20 ("matrix displays are well known in the art, where pixels are illuminated using matrix addressing as illustrated in FIG. 1.").

The select lines (i.e., "selection lines") "control[] the operational state of the "writing control section" (i.e., transistor P4 445) using "writing control signals." (i.e. High and

Low). For example, Dawson discloses that the select line 420 controls the operational state of transistor P4 445 by modifying the voltage (i.e. the writing control signal) that is applied to the gate of transistor P4 445 in order to turn transistor P4 445 on or off. Ex. 15, 8:33 ("The select line 420 is then set to 'Low'"'), 9:20-21 ("The select line 420 is then set to 'High'"').

With regard to claim 11, further teaching ***(f)*** **hold lines in which voltage control signals for controlling the operation state of the voltage control sections of the display pixels are applied**;

Referring to Fig. 4 below, Dawson discloses an auto zero 440 that is connected to the gate of transistor P3 465. Ex. 15, 8:13—14. Dawson's auto zero line is the claimed "hold line."

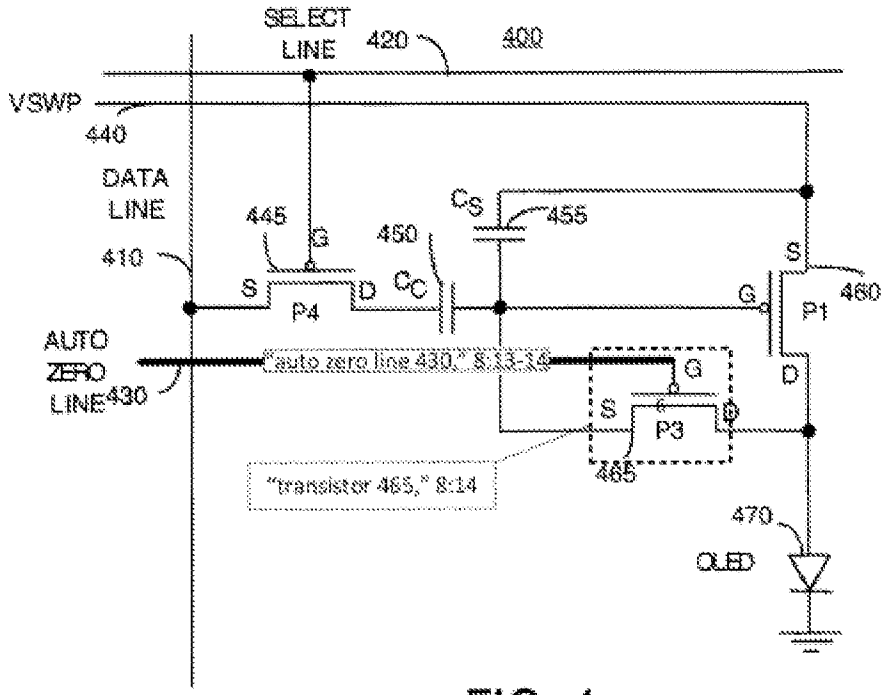


FIG. 4

Ex. 15, Fig. 4 (annotations added). Dawson discloses that its displays will have a plurality of pixels arranged in an array. Id., 3:33—35 ("Although the present invention is illustrated below as a single pixel or pixel structure, it should be understood that the pixel can be employed with other pixels, e.g., in an array, to form a display."). Accordingly, Dawson discloses a plurality of hold lines, one for each row of pixels. Id., Fig. 1, 1:19-20 ("matrix displays are well known in the art, where pixels are illuminated using matrix addressing as illustrated in FIG. 1.").

The auto zero lines (i.e., "hold lines") "control[] the operational state of the voltage control section" (i.e., transistor P3 465) using "voltage control signals." (i.e. High and Low). For example, Dawson discloses that the auto zero line 430 controls the operational state of transistor P3 465 by modifying the voltage (i.e., voltage control signal) that is applied to the gate of transistor P3 465 in order to turn transistor P3 465 on or off. Ex. 15, 8:30-32 ("Auto Zero line 430 is then set to 'Low'"'), 9:2-3 ("Auto Zero line 430 is then set to 'High'').

With regard to claim 11, further teaching ***(h)*** **data lines to which the gradation sequence signals are supplied**; As discussed in Section IX.A.6 of the Request, Dawson discloses "data lines" under either previously asserted construction.

Referring to Fig. 4 below, Dawson discloses a data line 410. Ex. 15, 8:11-12.

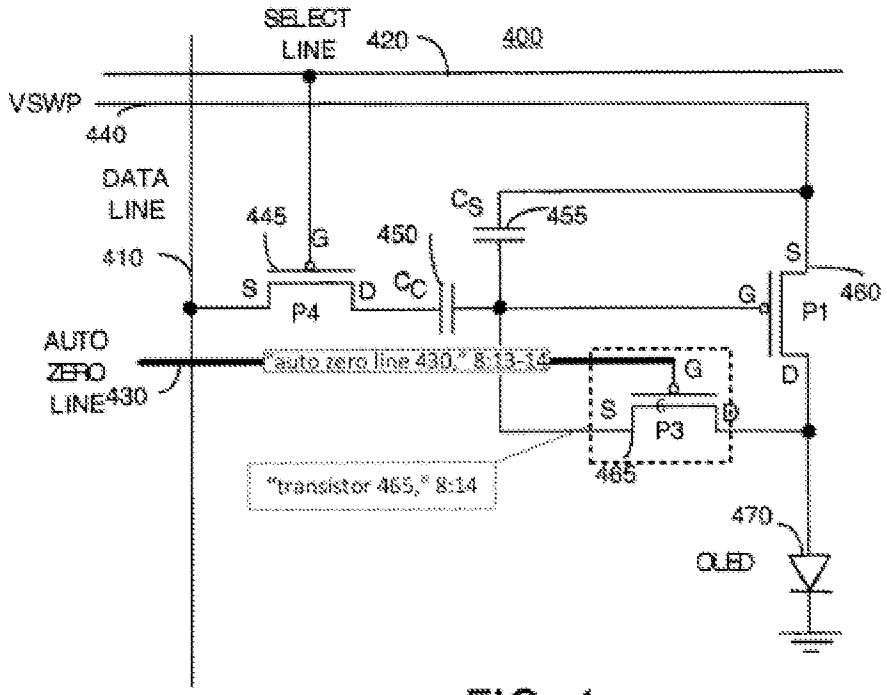


FIG. 4

Ex. 15, Fig. 4 (annotations added). Dawson discloses that its displays will have a plurality of pixels arranged in an array. Id., 3:33-35 ("Although the present invention is illustrated below as a single pixel or pixel structure, it should be understood that the pixel can be employed with other pixels, e.g., in an array, to form a display."). Accordingly, a plurality of data lines would be used, one for each column of pixels. Id., Fig. 1, 1:19-20 ("matrix displays are well known in the art, where pixels are illuminated using matrix addressing as illustrated in FIG. 1.").

The data lines 410 ("data lines") further supply a "gradation sequence signal" in the form of data voltage to the writing control sections (transistor 445) of the various pixels. Ex. 15, 9:10-12 ("Next, the data line is then switched from a reference voltage to a lower voltage (data voltage) where the change in the data is referenced to the data.").

With regard to claim 11, further teaching ***(i)* a selection driver which applies the writing control signals in the selection lines;** As discussed above in connection with limitation [11f], Dawson discloses applying "writing control signals" to "selection lines." Ex. 15, 8:33 ("The select line 420 is then set to 'Low"), 9:20-21 ("The select line 420 is then set to 'High'"').

Dawson discloses that the writing control signals need to change from a low value to a high value at different stages of the operation of Dawson's Fig. 4 embodiment. Id 8:33 ("The select line 420 is then set to 'Low and a 'reference voltage' is applied on the data line 410."), 9:20 ("The select line 420 is then set "High").

Dawson also discloses that the embodiment of Fig. 4 includes additional circuitry to implement its teachings, as described in Fig. 5 of Dawson. Ex. 15, 3:7-9 ("FIG. 5 depicts a block diagram of a system employing a display having a plurality of active matrix LED pixel structures of the present invention.").

Dawson discloses that the circuitry resides in pixel interface 522. Ex. 15, 13:22—23 ("the pixel interface 522 contains the necessary circuitry to drive the pixels... 400.")

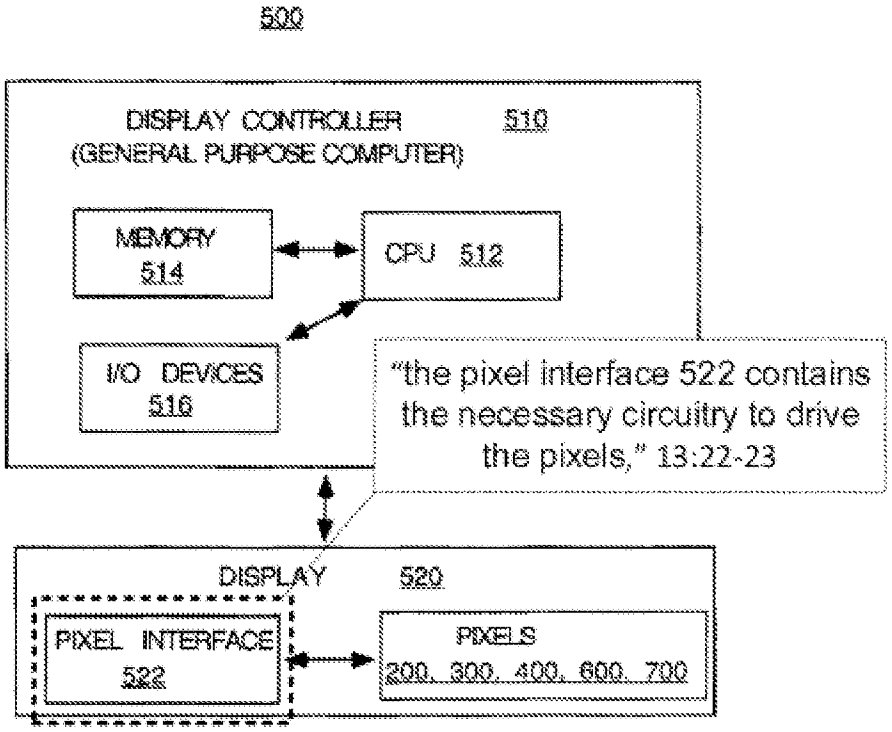


FIG. 5

Ex. 15, Fig. 5 (annotations added)

While Dawson does not expressly disclose that the "writing control signals" are applied to the "selection lines" by circuitry residing within pixel interface 522 (i.e., a "selection driver'), a POSITA would have had reason to do so, for at least the following reasons.

First, a POSITA looking to implement the teachings of Fig. 4 of Dawson would understand that it would require additional circuitry to "drive" the pixels, and that in order to drive the pixels, it would be necessary to apply different voltages to the gate of transistor P4 445. Ex. 15, 8:33, 9:20-21. Ex. 19, ¶¶ [0060]—[0061].

Second, a POSITA would understand that a driver circuit was a well-known and conventional technique used to transmit control signals to transistors in order to modify their operational states. Ex. 19, ¶¶ [0027]-[0030], ¶ [0062]; Ex. 18 at 72 ("Electrically, the OLED's drive requirements are so similar to those of the LCD that it is expected that many LCD production lines could be converted to OLED production in a reasonably straightforward and economical manner.").

Thus, implementing the claimed selection driver to apply the writing control signals to the hold lines, as claimed, would be nothing more than combining prior art elements (i.e., a driver circuit and the embodiments described in Fig. 4 of Dawson) according to known methods to yield predictable results. M.P.E.P. § 2143; KSR, 550 U.S. at 415-421; Ex. 15, 8:33, 9:20-21, 13:22-23,; Ex. 19, ¶¶ [0058]-[0063].

Implementing a driver circuit with Dawson's Fig. 4 embodiment would be nothing more than applying a known technique (i.e., a driver circuit) to a known device (i.e., select line 420 described in Fig. 4 of Dawson) to yield predictable results (i.e., the operational state of transistor P4 445 being controlled by the signals sent by the driver circuit). M.P.E.P. § 2143; KSR, 550 U.S. at 415-421: Ex. 15, 8:33, 9:20-21, 13:22-—23; Ex. 19, ¶¶ [0058]-[0063].

A POSITA would also have a reasonable expectation of success implementing a selection driver to apply writing control signals to selection lines because it was a well-

known technique with predictable results—it would supply the writing control signals at the appropriate timing as explained in Dawson's discussion of Fig. 4. M.P.E.P. § 2143; KSR, 550 U.S. at 415-421; Ex. 15, 8:33, 9:20—21, 13:22—23; Ex. 19, ¶ [0063].

With regard to claim 11, further teaching ***(j)* a hold driver which applies the voltage control signals in the hold lines**; and as discussed above in connection with limitation [11g], Dawson discloses applying voltage control signals to hold lines. Ex. 15, 8:30—32 ("Auto Zero line 430 is then set to 'Low'"), 9:2-3 ("Auto Zero line 430 is then set to 'High'").

Dawson discloses that the voltage control signals need to change from a "low" value to a "high" value at different stages of the operation of Dawson's Fig. 4 embodiment. Ex. 15, 8:30-32, 9:2-3, 9-10.

Dawson also discloses that it's embodiment of Fig. 4 includes additional circuitry to implement its teachings, as described in Fig. 5 of Dawson. Ex. 15, 3:7-9 ("FIG. 5 depicts a block diagram of a system employing a display having a plurality of active matrix LED pixel structures of the present invention."). 'Dawson discloses that the circuitry resides in pixel 'interface 522. Ex. 15, 13:22—23 ("the pixel interface 522 contains the necessary circuitry to drive the pixels … 400.")

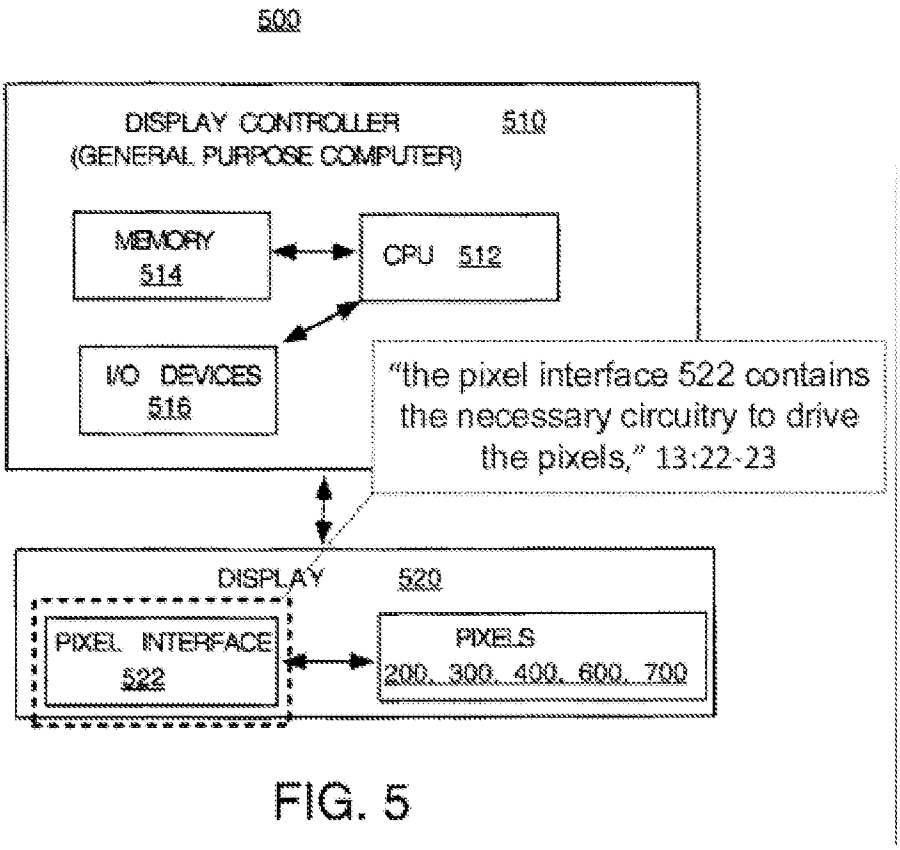


FIG. 5

Ex. 15, Fig. 5 (annotations added)

While Dawson does not expressly disclose that the "voltage control signals" are applied to the "hold lines" by circuitry residing within pixel interface 522 (i.e... a "hold driver') a POSITA would have had reason to do so, for at least the following reasons.

First, a POSITA looking to implement the teachings of Fig. 4 of Dawson would understand that it would require additional circuitry to "drive" the pixels, and that in order to drive the pixels, it would be necessary to apply different voltages to the gate of transistor P3 465. Ex. 15, 8:30-32, 9:2—3, 9-10; Ex. 19, ¶¶ [0066]-[0067].

Second, a POSITA would understand that a driver circuit was a well-known and conventional technique used to transmit control signals to transistors in order to modify their operational states. Ex. 19, ¶¶ [0027]-[0030], ¶ [0068]; Ex. 18 at 72 ("Electrically, the OLED's drive requirements are so similar to those of the LCD that it is expected that many LCD production lines could be converted to OLED production in a reasonably straightforward and economical manner.").

Thus, implementing the claimed hold driver to apply the voltage control signals to the hold lines, as claimed, nothing more than combining prior art elements (i.e., a driver circuit and the embodiments described in Fig. 4 of Dawson) according to known methods to yield predictable results. M.P.E.P. § 2143; Ex. 15, 8:33, 9:20-21, 13:22-23; Ex. 19, ¶¶ [0064]-[0069].

Implementing a driver circuit with Dawson's Fig. 4 embodiment would be nothing more than applying a known technique (i.e., a driver circuit) to a known device (i.e., auto zero line 420 described in Fig. 4 of Dawson) to yield predictable results (i.e., the operational state of transistor P3 465 being controlled by the signals sent by the driver circuit). M.P.E.P. § 2143; Ex. 15, 8:33, 9:20-21, 13:22-23; Ex. 19, ¶¶ [0064]-[0069].

A POSITA would also have a reasonable expectation of success implementing a signals to hold lines because it was a well-known technique with predictable results it

would supply the voltage control signals at the appropriate timing as explained in Dawson's discussion of Fig. 4. M.P.E.P. § 2143; Ex. 15, 8:33, 9:20-21, 13:22-23; Ex. 19, ¶ [0069].

With regard to claim 11, further teaching ***(k)* a data driver which supplies the gradation sequence signals to the data lines**; As discussed above in connection with limitation [11h], Dawson discloses supplying "gradation sequence signals to the data lines." Ex. 15, 9:10-12 ("Next, the data line is then switched from a reference voltage to a lower voltage (data voltage) where the change in the data is referenced to the data.").

Dawson discloses that the gradation signals are only supplied to the data during certain periods of time during the different stages of the operation of Dawson's Fig. 4 embodiment. Id., 9:10—12 ("Next, the data line is then switched from a reference voltage to a lower voltage (data voltage) where the change in the data is referenced to the data.").

Dawson also discloses that it's embodiment of Fig. 4 includes additional circuitry to implement its teachings, as described in Fig. 5 of Dawson. Id., 3:7-9 ("FIG. 5 depicts a block diagram of a system employing a display having a plurality of active matrix LED pixel structures of the present invention.")

Dawson discloses that the circuitry resides in pixel interface 522. Ex. 15, 13:22—23 ("the pixel interface 522 contains the necessary circuitry to drive the pixels . . . 400.").

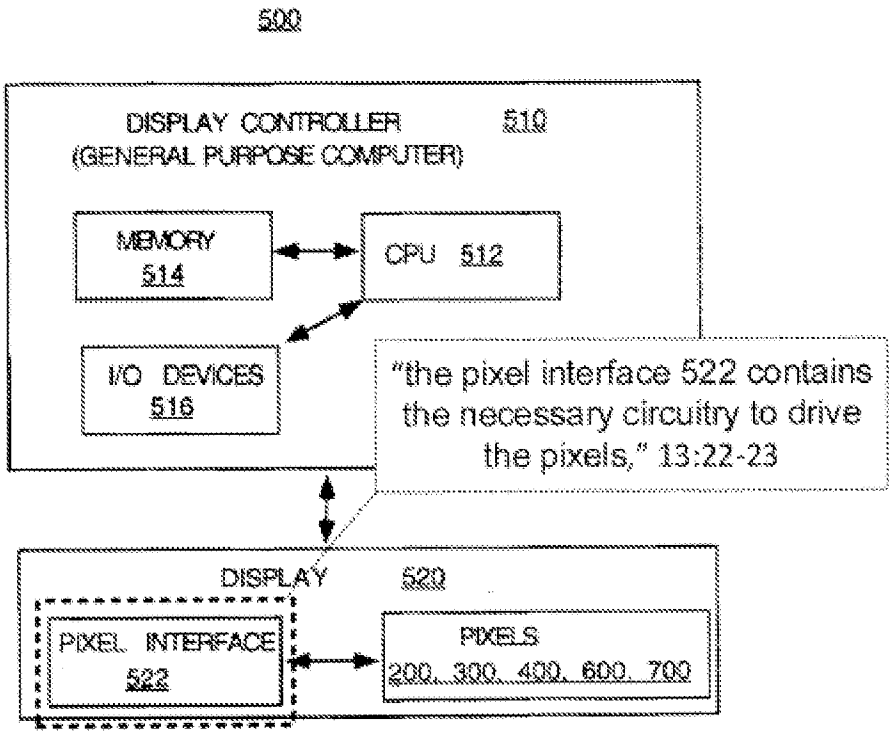


FIG. 5

Ex. 15, Fig. 5 (annotation added)

While Dawson does not expressly disclose that the "gradation sequence signals" are applied to the "data lines" by circuitry residing within pixel interface 522 (i.e., a "data driver') a POSITA would have had reason to do so, for at least the following reasons.

First, a POSITA looking to implement the teachings of Fig. 4 of Dawson would understand that it would require additional circuitry to drive the pixels, and that in order

to drive the pixels, it would be necessary to apply gradation sequence signals to the data line to control the illumination of Dawson's OLED. Ex. 15, 9:10-12, 9:24-34: Ex. 19, ¶¶ [0072]-[0073].

Second, a POSITA would understand that a data driver circuit was a well-known and conventional technique used to transmit gradation sequence signals for controlling the illumination of light emitting elements, such as Dawson's OLED. Dawson, 9:10-12, 9:24-34; Ex. 19, ¶¶ [0027]-[0030], ¶ [0068]; Ex. 18 at 72 ("Electrically, the OLED's drive requirements are so similar to those of the LCD that it is expected that many LCD production lines could be converted to OLED production in a reasonably straightforward and economical manner.").

Thus, implementing the claimed data driver to apply the gradation sequence signals to the data lines, as claimed, would be obvious because it is nothing more than combining prior art elements (i.e., a driver circuit and the embodiments described in Fig. 4 of Dawson) according to known methods to yield predictable results. M.P.E.P. § 2143; KSR, 550 U.S. at 415-421; Ex. 15, 9:10-12, 9:24—34; Ex. 19, ¶¶ [0070]-[0075].

Implementing a driver circuit with Dawson's Fig. 4 embodiment would be nothing more than applying a known technique (i.e., a driver circuit) to a known device (i.e., data line 410 described in Fig. 4 of Dawson) to yield predictable results (i.e., the illumination level of Dawson's OLED being controlled by the signals sent by the driver circuit). M.P.E.P. § 2143; KSR, 550 U.S. at 415-421; Ex. 15, 9:10-12, 9:24-34; Ex. 19, ¶¶ [0070]-[0075].

A POSITA would also have a reasonable expectation of success implementing a data driver to supply gradation sequence signals to data lines because it was a well- known technique with predictable results—it would supply the gradation sequence signals at the appropriate timing as explained in Dawson's discussion of Fig. 4. M.P.E.P. § 2143; KSR, 550 U.S. at 415-421; Ex. 15, 9:10-12, 9:24-34; Ex. 19, ¶ [0075].

With regard to claim 11, further teaching ***(l)*** **wherein, with respect to each of the display pixels, the data driver applies a precharge voltage exceeding a threshold value of the drive transistor to the data line, and the light emission drive circuit applies the precharge voltage applied to the data line to the electric charge accumulating section via the writing control section,** Dawson teaches this limitation. For convenience, limitation [11] is addressed in three parts below.

Note: the '615 Patent specification refers to two separate 'precharge voltages' (see column 19 line 33 through column 20, line 67):

(1) the precharge voltage applied to the data line;

(2) the precharge voltage measured between the opposite ends of the electric charge accumulation section that exceeds a threshold value of the drive transistor.

<u>ii Dawson teaches that the "data driver applies a precharge voltage . . . to the data line."</u>

First, Dawson discloses a "precharge voltage" that is applied to the data line in the form of a reference voltage. Ex. 15, 8:33-34 ("a 'reference voltage' is applied on the data line 410. The reference voltage can be arbitrarily set, but it must be greater than the highest data voltage."). Dawson's reference voltage is applied to the data line before Dawson's "data voltage" (i.e., the claimed gradation sequence signal). Id., 9:9—12 ("At the end of the Auto Zero phase . . . the data line was at a 'reference voltage'. Next, the data line is then switched from a reference voltage to a lower voltage (data voltage).").

As discussed above in connection with limitation [11k], Dawson also teaches a data driver (i.e., circuitry residing in pixel interface 522) that supplies a data voltage (i.e., "gradation sequence signal") and a reference voltage (i.e., "precharge voltage"). Ex. 15, 9:10—12 ("Next, the data line is then switched from a reference voltage to a lower voltage (data voltage) where the change in the data is referenced to the data.").

ii. Dawson discloses that the precharge voltage "exceeds the threshold value of the drive transistor."

Dawson discloses that the precharge voltage "exceed[s] a threshold value of the drive transistor." Specifically, Dawson discloses applying a precharge voltage higher than the highest data voltage and then allowing the circuit to settle down to the threshold value of transistor P1 460 (i.e., the "drive transistor'). Ex. 15, 8:33-34 ("The reference voltage can be arbitrarily set, but it must be greater than the highest data voltage."), 9:1-2 ("The pixel circuit is now allowed to settle to the threshold of

transistor P1 460.").

Dawson further discloses an implementation using NMOS transistors. Ex. 15, 13:32-14:3. In such an implementation, transistor 460 would turn on only when a voltage higher than its threshold voltage is applied between its gate and source. Id., 13:32-14:3. This further demonstrates that the reference voltage would need to exceed the threshold value of transistor 460. Id., 8:24—9:6.

iii. Dawson "applies the precharge voltage applied to the data line to the electric charge accumulating section via the writing control section."

Referring Fig. 4 below, Dawson discloses that the reference voltage is applied to the data line 410. Ex. 15, 8:32—33. Dawson furthers discloses that during the auto-zero phase, the select line 420 is set so that transistor P4 445 (i.e., the writing control section) is turned on. Id. When transistor P4 445 is turned on, the reference voltage is applied to the electric charge accumulating section. See also Ex. 15, 9:3-6 ("The effect of this Auto Zero phase is to store on the capacitor Cc 450 a voltage (an auto-zero voltage) that represents the difference between the reference voltage on the data line and the transistor threshold voltage of PI 460.").

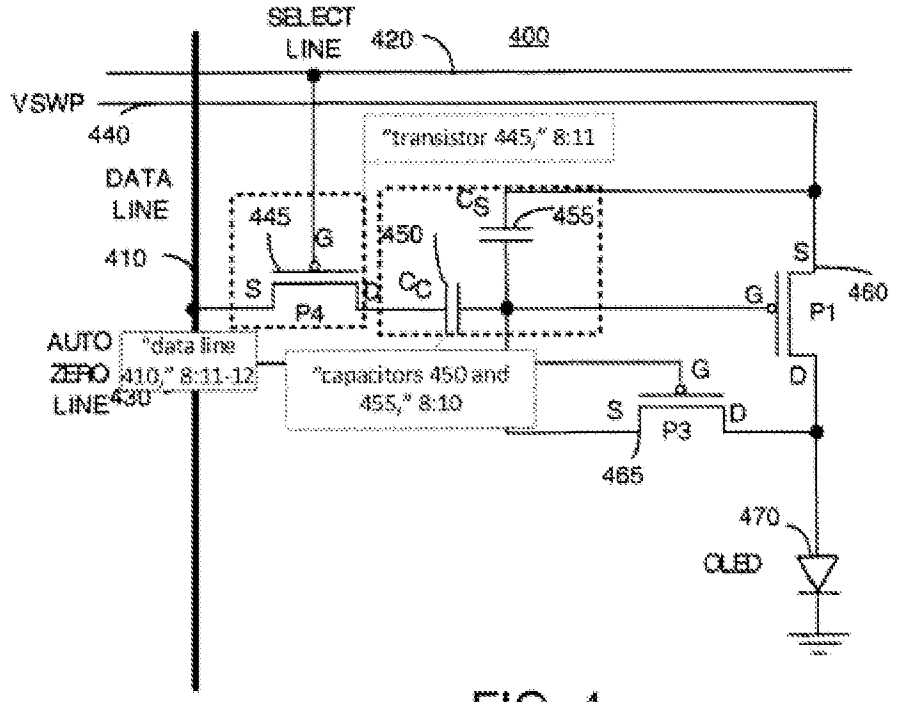


FIG. 4

Ex. 15, Fig. 4 (annotations added).

With regard to claim 13, further teaching ***wherein the precharge voltage and the gradation sequence signal applied from the data driver to the data line are applied in the electric charge accumulating section via the writing control section at different timings, respectively,*** As described above in connections with limitations [11b], [11d], [11h], and [11k], Dawson discloses that a "data driver" applies a "gradation sequence signal' (i.e., a data voltage in Dawson) to the data line, and that the gradation sequence signal is applied to the electric charge accumulation section via the writing control section.

Also, as described above in connection with limitation [11l], Dawson discloses that a data driver applies a "precharge voltage" (i.e., a reference voltage in Dawson) to the data line, and that the precharge voltage is applied to the electric charge accumulation section via the writing control section.

Dawson discloses that the precharge voltage and gradation sequence signals are applied at different respective timings. First Dawson applies a reference voltage (i.e., precharge voltage), as part of its Auto-Zero phase. Ex. 15, 8:32-33 ("The select line 420 is then set to 'Low' and ta 'reference voltage is applied on the data line 410."). After the Auto-Zero phase is complete.,. Dawson disclose that the data voltage (i.e., gradation sequence signal) is applied. Id., 9:9-12 ("At the end of the Auto Zero phase, . . . the data line was at a 'reference voltage'. Next, the data line is then switched from a reference voltage to a lower voltage (data voltage).").

Response to Arguments

Applicant's arguments filed in the Patent Owner's Statement of 12/17/2021 and 3PR comments have been fully considered but they are not persuasive.

Patent Owner argues that ***neither Kimura I... nor Dawson... teaches or suggests "the data driver applies a precharge voltage exceeding a threshold value of the drive transistor to the data line."***

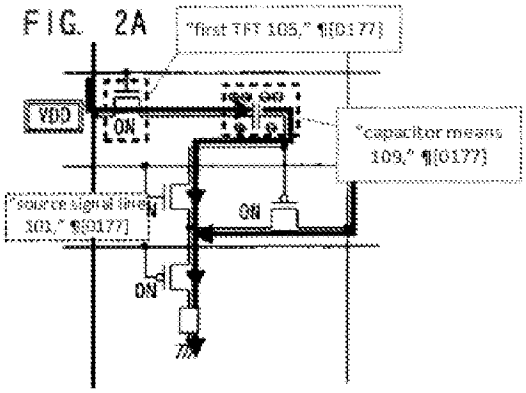
But then specifically admits that "in Kimura I, VDD is a voltage level that is greater than Vth." (see page 2, line 6)

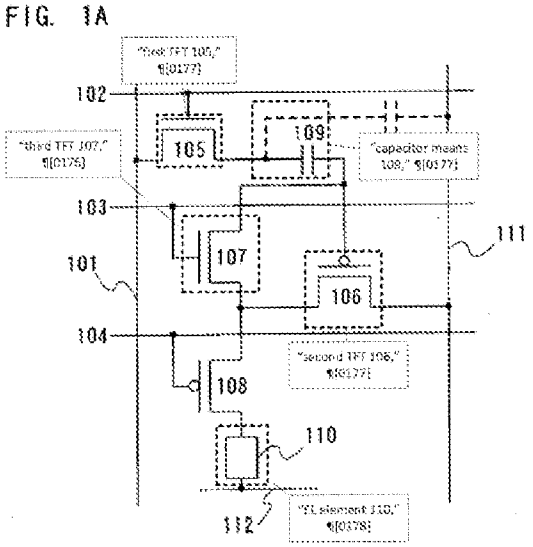
This seems to be a clear admission that the precharge voltage applied to the data line exceeds the threshold value of the drive transistor.

Patent Owner argues that ***"In Kimura I, the second TFT 106 is a p-channel transistor. It is well known in the art that the threshold value of a p-channel transistor is a negative voltage, and the transistor is "turned - on" only when the applied voltage is more negative than the negative threshold voltage Vth. In other words, for a given voltage V to "exceed[] a threshold value" (Vth) of" a p-channel transistor, that voltage level must be sufficiently negative, such that V is less than Vth.***

Moreover, in Kimura I, VDD is a voltage level that is greater than Vth. Specifically, VDD is applied to the left side of "capacitor means 109," as shown

by Requester's annotation of Kimura I's Fig. 2A (reproduced below). As shown in the below diagram, the application of positive voltage VDD to the left side of capacitor means 109 and allowing current to flow between the right side of capacitor means 109 and the EL element 110 accumulates a negative electric charge on the right side of capacitor means 109, which results in a voltage less than VDD being applied to the gate of TFT 106. But VDD (..e., the alleged "precharge voltage") itself is a positive voltage"

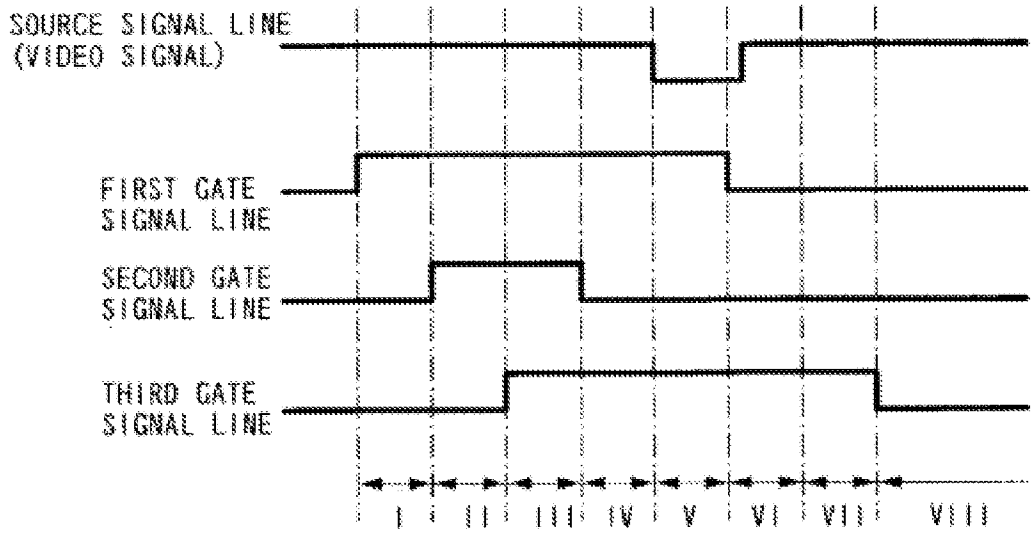




In response, the Examiner submits that given the Patent Owner's reasoning "second TFT 106" would never be turn on, which is simply not the case. Given alone the figure 2A supplied in arguing this point shows flow through the on TFT 106. Further description supplied from the specification from paragraph 180 shows ***"as shown in FIG. 2A, the capacitor mean 109 is charged, and when a voltage held by the capacitor means 109 exceeds a threshold value (Vth) of the second TFT 106, the***

second TFT is turned ON." The fact that Kimura I explicitly states that the "***voltage ... exceeds a threshold value (Vth) of the second TFT 106"*** seems particularly relevant to the claimed limitation of "a precharge voltage exceeding a threshold value of the drive transistor". It appears that the Patent Owner is trying to impart some other meaning to the term 'exceeds' other than (1) its broadest reasonable interpretation, (2) the Patent's specification, and (3) the context of the claim. Kimura I fully describes what it takes to turn second TFT 106 on, noting "***In a P-channel TFT when an L level is inputted to the gate electrode, it is turned ON.***" (see paragraph 179) Noting further that "***a potential of the gate electrode of the second TFT 106 become a potential obtained by adding the threshold value Vth to the potential of the video signal Vdata inputted from the source signal line 101. Here, the TFT106 is a P-Channel type and the threshold value Vth is a negative value. This, the potential actually becomes a value smaller than Vdata by the absolute value of Vth . Accordingly, the second TFT 106 is turned ON (section V)***". (see paragraph 183) As can be seen from figure 1B below, section V is where the video signal Vdata goes Low.

FIG. 1B



Patent Owner argues that "***Because TFT 106 has a negative threshold voltage that can only be "exceeded" by a voltage that is less than this threshold voltage, Kimura I's disclosure of positive VDD thus cannot constitute the claimed "precharge voltage exceeding a threshold value of the drive transistor***."

In response, the Examiner respectfully submits that the reference explicitly states that the precharge "***voltage held by the capacitor means 109 exceeds a threshold value (Vth) of the second TFT 106",*** then goes on to show multiple examples of flow occurring through second TFT 106. Note, the precharge voltage VDD is applied to the signal lines and when the second TFT 106 is turned on the video signal inputted is Vdata not VDD, where VDD > Vdata. (see paragraphs 25 and 183).

With regard to arguments directed at Dawson, Patent Owner uses the same flawed reasoning and interpretation of the term 'exceeding' as used in arguing against Kimura I. Again Dawson uses p-type transistors, which have a negative threshold. In Dawson's system a positive voltage is again applied to the reference voltage which according to the ordinary meaning (as presented in the 3PR supplied dictionary references) exceeds the threshold voltage. Now again, similar to Kimura I, transistor 460 in Dawson has further circuit elements and processing done on the signal prior to it reaching the gate terminal of the transistor (see figure 4 of Dawson, Ex. 15, 8:33-34).

Requester further admits that Dawson appreciated the use of n-type transistors alternately, but argues that if this where the case "the system would need to apply a positive voltage on the right side of capacitor 450, which would be done through the application of a negative reference voltage on the data line 410." Arguing the converse this way shows that the Patent Owner fully appreciated the processing of the signal that takes place across other circuit elements between the data drive applied voltage and what reaches the drive transistor.

Summary

Claims 11-13 are REJECTED.

Claims 1-10 and 14-15 are not subject to reexamination.

Conclusion

Extensions of time under 37 CFR 1.136(a) do not apply in reexamination proceedings. The provisions of 37 CFR 1.136 apply only to "an applicant" and not to parties in a reexamination proceeding. Further, in 35 U.S.C. 305 and in 37 CFR 1.550(a), it is required that reexamination proceedings "will be conducted with special dispatch within the Office."

The patent owner is reminded of the continuing responsibility under 37 CFR 1.565(a) to apprise the Office of any litigation activity, or other prior or concurrent proceeding, involving the patent throughout the course of this reexamination proceeding. The requester is also reminded of the ability to similarly appraise the Office of any such activity or proceeding throughout the course of this reexamination proceeding. See MPEP § § 2207, 2282, and 2286.

All correspondence relating to this *ex parte* reexamination proceeding should be directed:

By Mail to: Mail Stop Ex Parte Reexam
Central Reexamination Unit
Commissioner for Patents
United States Patent & Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

By FAX to: (571) 273-9900

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Any inquiry concerning this communication or earlier communications from the Reexamination Legal Advisor or Examiner, or as to the status of this proceeding, should be directed to the Central Reexamination Unit at telephone number (571) 272-7705.

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